CAT.No.1D0401-1.0E

Control IC

for quasi-resonant power supply

MS1007SH *Application Note*

The product and product specifications are subject to change

SHINDENGEN

SHINDENGEN ELECTRIC MFG. CO. , LTD

CAT.No.1D0401-1.0E

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Caution		Improper handling may result in minor injury or property damage.

Warning		This IC is intended to be used for general electronic equipment (office equipment, communication equipment, measurement equipment, consumer electronics, etc.). Do not use the product for medical equipment, aerospace planes, trains, transportation equipment (vehicles, ships, etc.), or nuclear power control systems that may directly affect human life or health in case of a malfunction or trouble. Contact us before using the product in applications other than general electronic equipment.
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		In the event of a problem, an excessive voltage may arise at an output terminal, or the voltage may drop. Anticipate these fluctuations and any consequential malfunctions or destruction and provide adequate protection for equipment, such as overvoltage or overcurrent protection.
		Check the polarity of the input and output terminals. Make sure they are properly connected before turning on power. <<Failure to do so may lead to failure of the protective element or generate smoke or fire.>>
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Contents

1. Overview

1.1 Introduction

The MS1007SH quasi-resonant circuit to reduce standby power, achieve high efficiency and low noise. The IC incorporate various functions to make it more user-friendly and to make it easier to design a power supply with fewer external components.

1.2 Characteristics

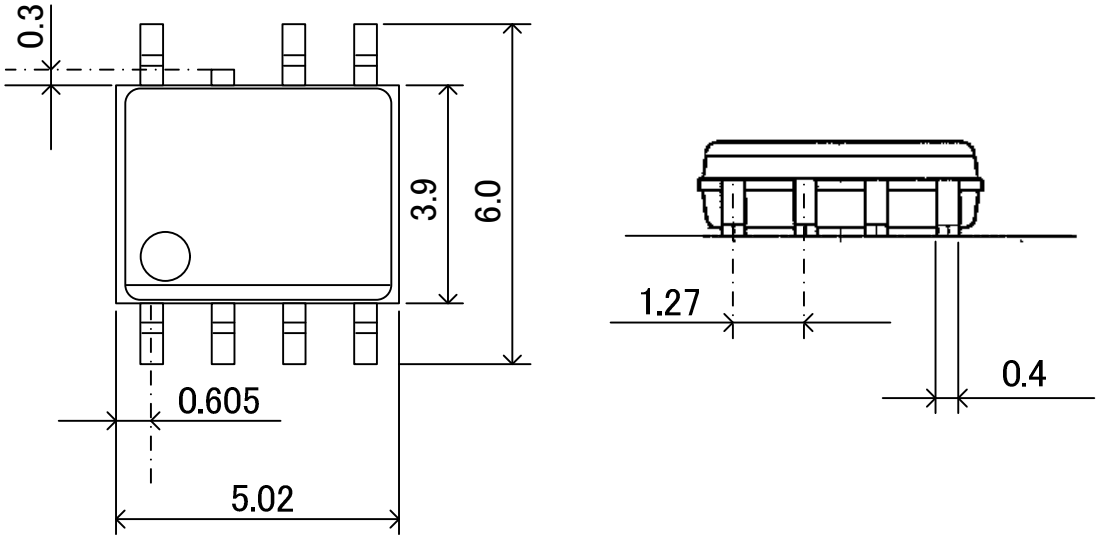
1) Quasi-resonant design for high efficiency and low noise
2) Four-Step soft-start function
3) Onboard startup circuit requires no startup resistor, dramatically reducing losses in the startup circuit.
4) The automatic bottom skip function controls increases in oscillation frequency and improves efficiency under light loads.
5) Auto burst function improves efficiency under light loads with no additional components.
6) Soft drive circuit reduces noise.
7) Thermal shutdown, overvoltage protection, and overload protection. (Auto-retry mode)
8) Primary current limit circuit incorporates an input voltage dependence correction circuit to reduce the number of components required.
9) Bias assist function for startup circuit
10) VCC-GND short circuit protection function
11) SOP-8/7J package employed for compact dimensions

1.3 Applications

Industrial equipment, video recorders, refrigerators, washing machines, air conditioners and other appliances in which standby power consumption is a design goal.

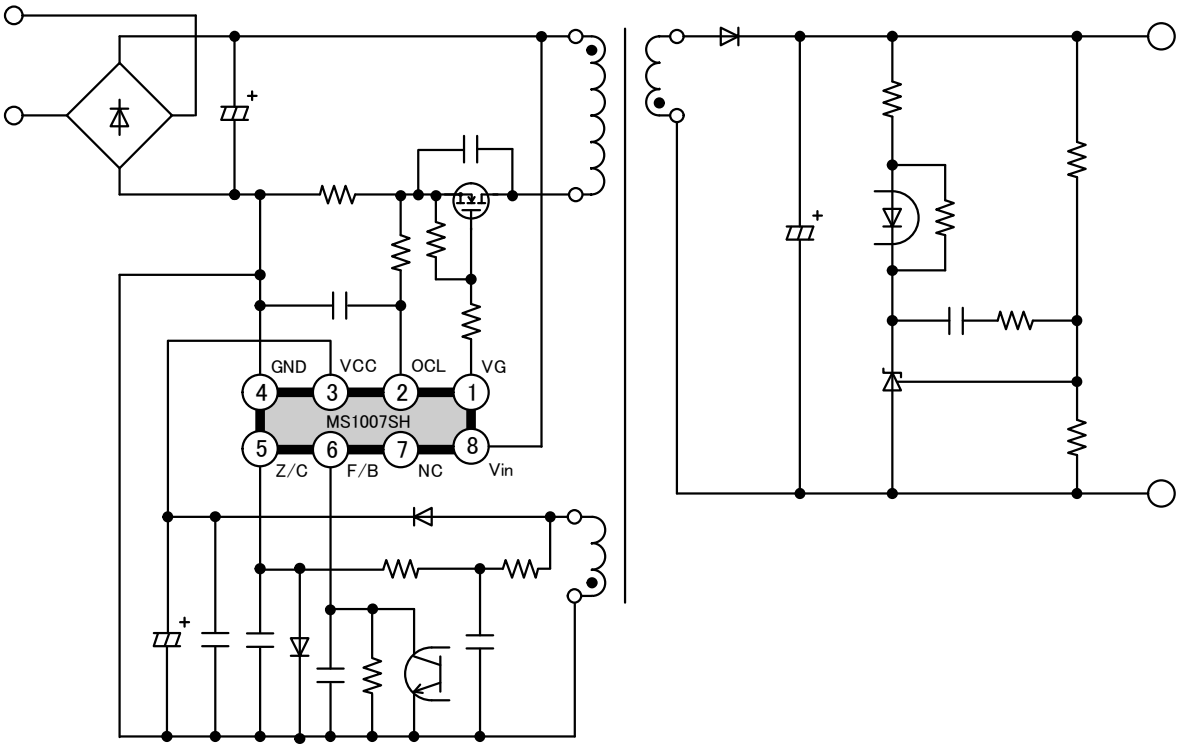
1.4 Appearance and dimensions

Unit: mm



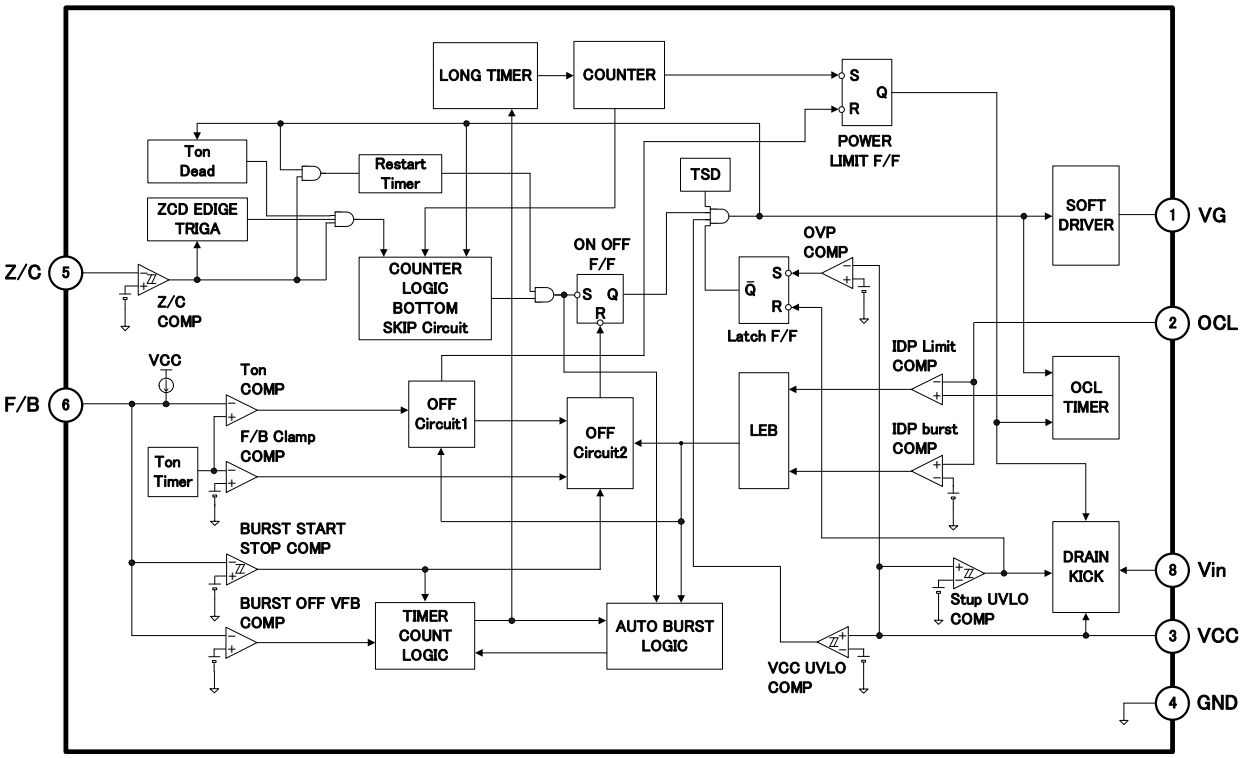
SOP-8/7J package

1.5 Basic circuit configuration

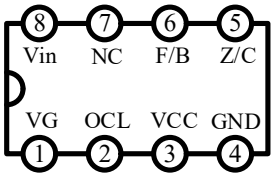


2. Block diagram

2.1 Block diagram



2.2 Pin names

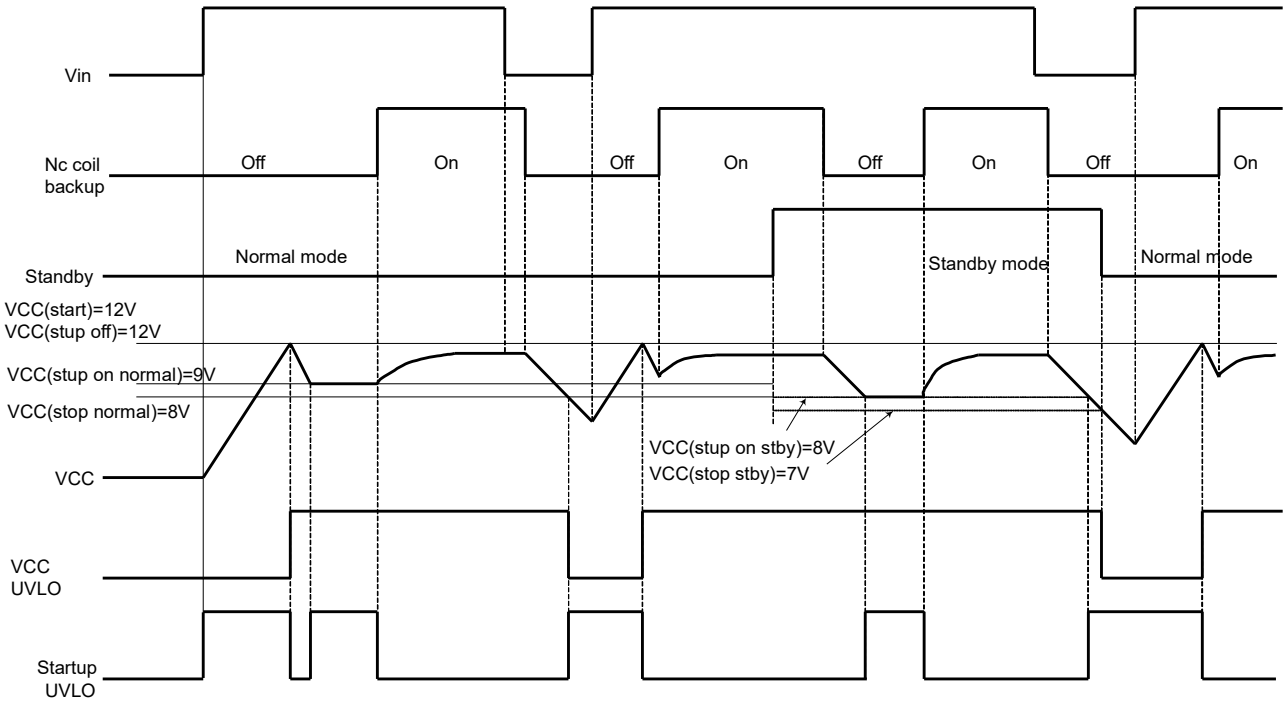


Pin number	Symbol	Pin name
1	VG	VG pin
2	OCL	Overcurrent limit pin
3	VCC	VCC pin
4	GND	Ground pin
5	Z/C	Zero current detection pin
6	F/B	Feedback signal input pin
7	NC	No connection
8	Vin	Vin pin

3. Circuit operation

3.1 Startup

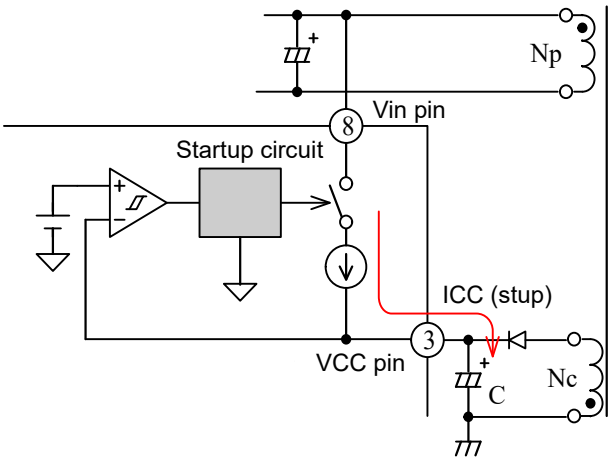
The diagram below shows the startup sequence.



Startup sequence

3.1.1 Startup circuit

The startup circuit does not require a startup resistor, making it possible to easily start the IC with a small number of components. A schematic diagram of the startup circuit is shown to the right.



Until the IC starts up, the startup circuit current ICC (stup) flows from the Vin pin to the VCC pin to charge C, as shown in the diagram.

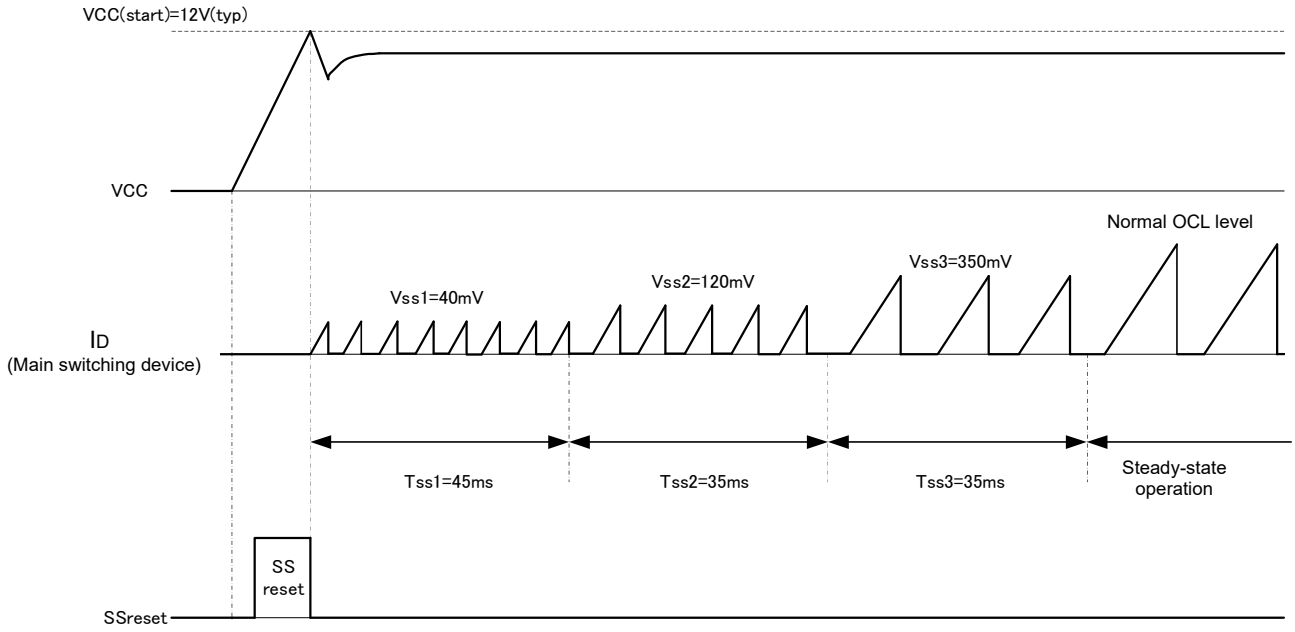
Oscillation begins when the voltage at the VCC pin : VCC reaches"On-State voltage" (VCC (start)) = 12V (typ). The startup circuit opens, and the startup circuit current stops. The VCC pin has hysteresis, which begins oscillating at VCC (start) and stops oscillating at "Under-Voltage lockout"(VCC (stop stby)) = 7V(typ) or (VCC (stop normal)) = 8V (typ).

A bias assist function is provided for the VCC voltage to ensure safe startup. For more information on the bias assist function, see Section 3.1.3.

3.1.2 Soft-start (SS)

At startup, the OCL level changes in four stages. Current flowing to the main switching device also increases in stages. The envelope curves of the current to the main switch are shaped in four steps to avoid abrupt switch startups.

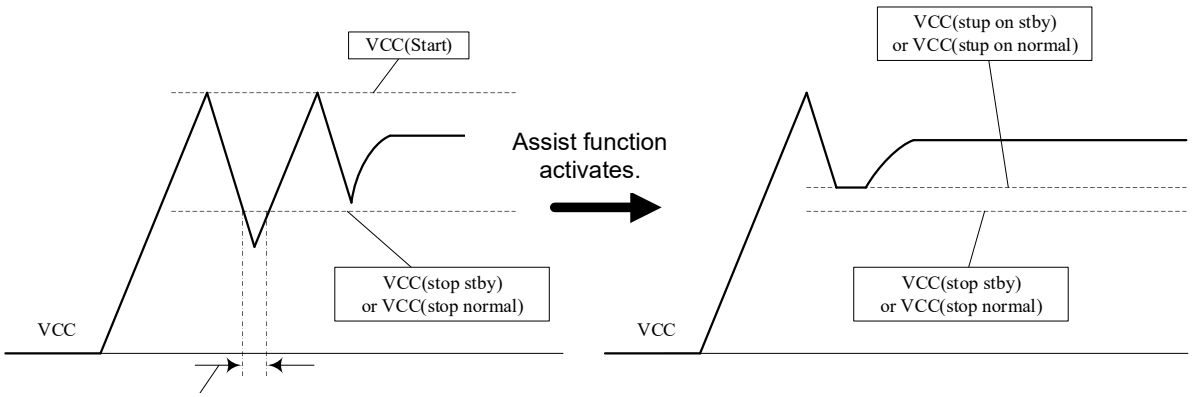
The soft start time depends on ''SS time'' (Tss1) to (Tss3) settings. The time settings are determined by the IC.



3.1.3 Bias assist

This IC incorporate an assist function to supply energy to VCC so that the voltage does not drop below ''Under-voltage lockout'' (VCC (stop stby)) = 7V(typ) or (VCC (stop normal)) = 8V(typ) to cause oscillation stop when it drops immediately after oscillation initiation at startup. This function eliminates the oscillation stop period at startup.

Shown below is a schematic diagram of VCC startup incorporating the bias assist function.



If the voltage drops below the oscillation stop voltage, oscillation halts, and the startup circuit must restart.

The voltage remains above the oscillation stop voltage to ensure that oscillation does not halt.

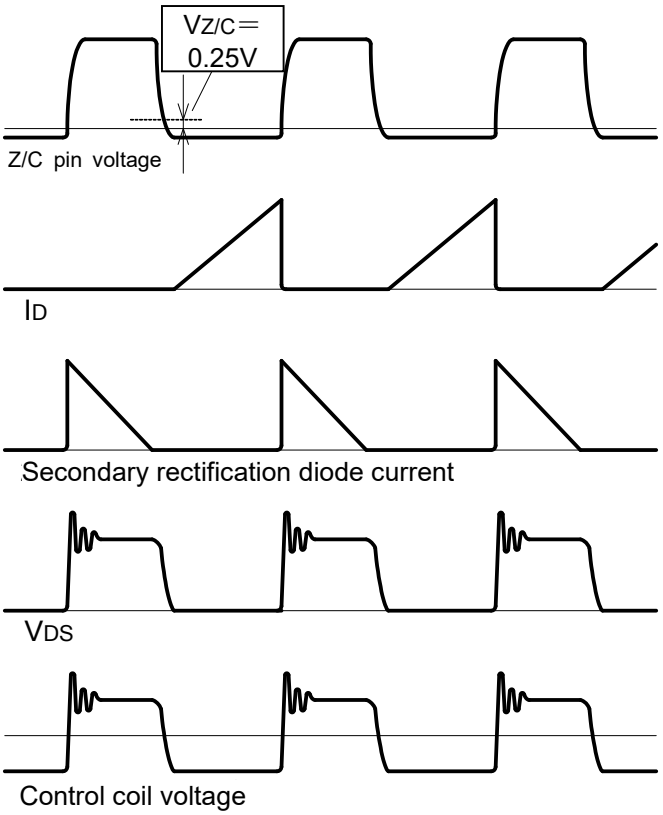
3.2 Oscillation

3.2.1 On-trigger circuit

As shown to the right, when a negative edge of Z/C pin voltage : $V_{Z/C}$ reaches "Zero current detection voltage" ($V_{Z/C}$) = 0.25V (typ), the gate signal is output, and the main switching device is turned on.

Current-critical operations are performed by detecting energy discharge timing with the control winding voltage : V_{NC} before turning on the main switching device.

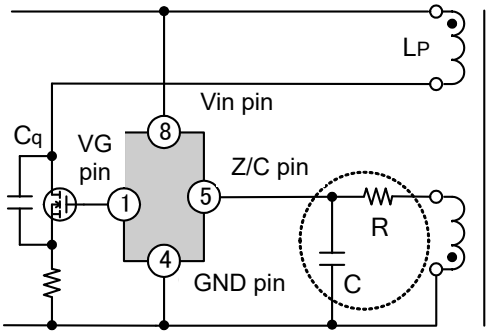
To minimize noise, negative edge detection detects a trigger while $V_{Z/C}$ falls from Hi to Low. The $V_{Z/C}$ = 0.25V incorporates 50mV hysteresis for improved noise resistance.



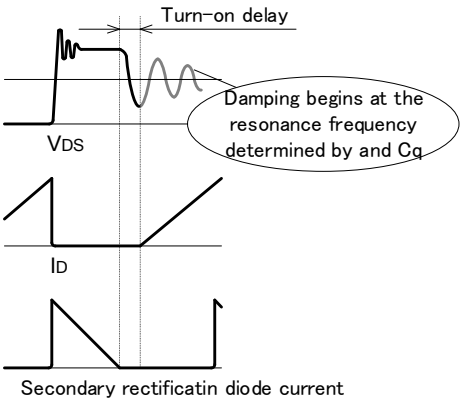
3.2.2 Quasi-resonance

In a circuit having resonating capacitor Cq between the drain and the source of the main switching device, as shown to the right, when the secondary diode current reaches 0 A, damping begins at the resonance frequency based on the primary inductance LP of the main transformer and the resonating capacitor.

Adjusting the time constant of the CR connected to the Z/C pin as shown on the right allows the main switching device to be turned on at a bottom of the damping voltage waveform, thereby reducing turn-on losses.



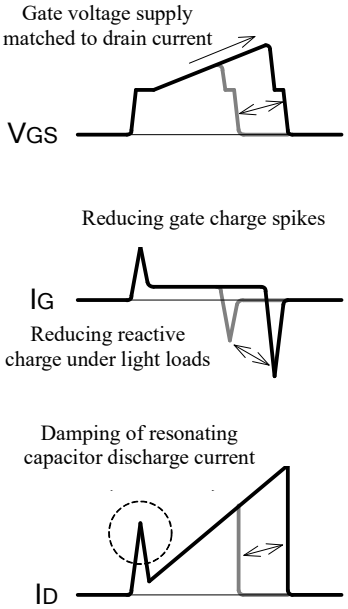
On-timing is delayed
With CR time constant



3.2.3 Soft drive

The soft drive circuit supplies a trigger voltage slightly greater than the gate threshold of the main switch as a gate drive voltage before constant voltage driving begins. After, this prevents the supply of greater gate voltage than necessary, because gate voltage supply matched to the drain current : ID.

The soft drive reduces losses by the gate charge voltage, reduces reactive charge under light loads and reduces noise by controlling the resonating capacitor discharge peak current.

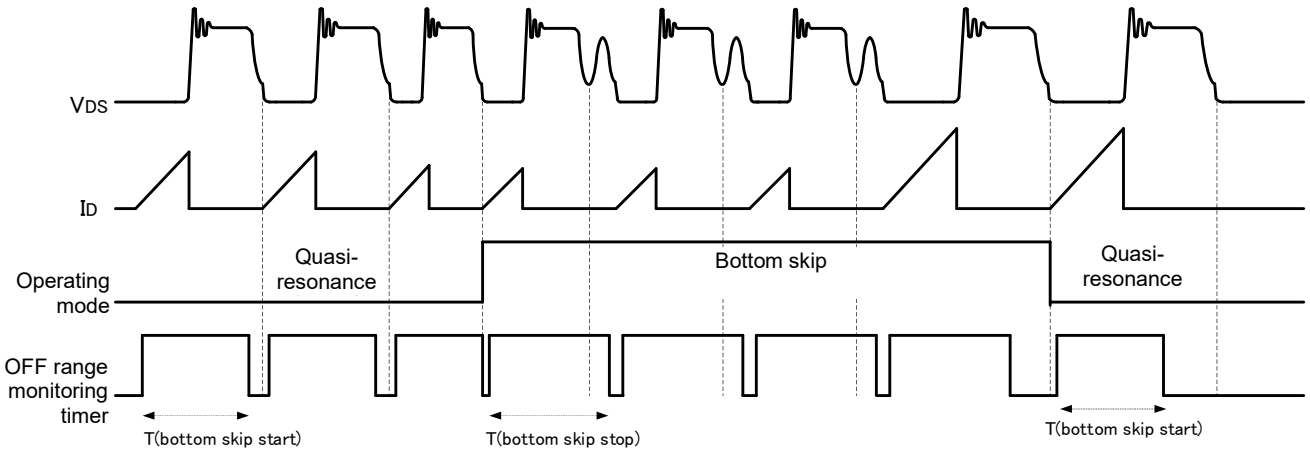


3.2.4 Bottom skip operation

The IC monitor the switching cycle. If the switching cycle length becomes shorter than “Bottom skip start time” (T (bottom skip start)) = 7.5μs (typ), the IC enter the following modes:

The IC switches from the normal quasi-resonance mode to the 1 bottom-skip mode (Turn-on at the second bottom).

In bottom-skip mode, the IC extends the off-period by a cycle of resonance. This controls an increase in the frequency. Once in bottom-skip mode, the off-time monitoring timer setting changes. When the time from turn-on to the first bottom becomes longer than “Bottom skip stop time” (T (bottom skip stop)) = 13μs (typ), the IC returns to normal quasi-resonance mode. Using hysteresis in this manner prevents jitter and acoustic noise.



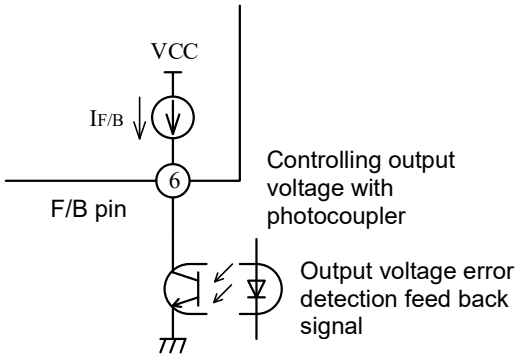
Sequence of the IC

3.2.5 Output voltage control

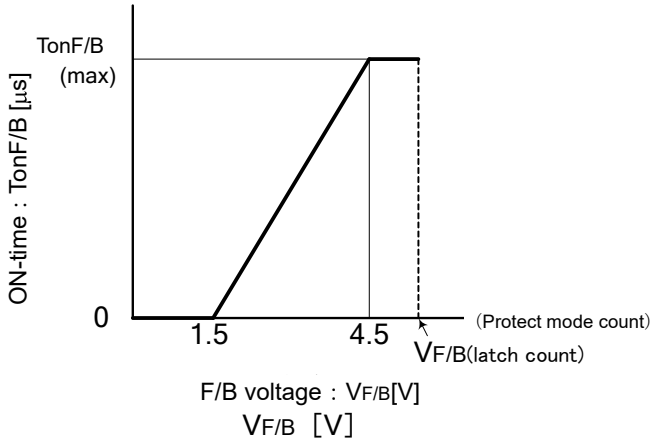
The IC control the output voltage : Vo with the on-time (TonF/B) proportional to the F/B Vref voltage : $V_{F/B}$.

TonF/B becomes “F/B Minimum on time” (TonF/B (min)) when $V_{F/B}$ is 1.5V, and “F/B Maximum on tome” (TonF/B Controlling output 2 (max)) when $V_{F/B}$ is 4.5V.

The F/B current : $I_{F/B}$ flows from the F/B pin. The Output voltage impedance of the photocoupler transistor externally error detection connected between the F/B pin and the GND pin is varied by feed back signal a control signal from the secondary output detection circuit, thereby controlling the on-time of the main switching device to produce a constant voltage.



“Timer Protect mode count start voltage” ($V_{F/B}$ (Protect mode count)) = 4.6V (typ) is set up for the F/B pin. When the voltage exceeds the set level, the timer begins counting. After maintaining this state for approximately 250ms (T (Protect mode count)), This IC shift to Overload protection mode.



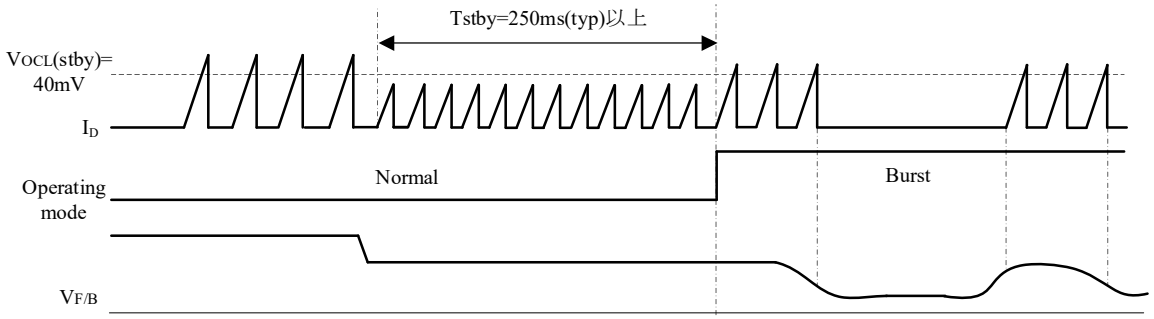
3.3 Burst mode oscillation

3.3.1 Auto-burst mode (Auto-Standby mode)

The IC switch between normal mode and burst mode automatically (auto-burst). This enables low standby power consumption with no other components required for standby mode.

1) Switching from normal mode to burst mode

The IC switches from normal mode to burst mode when the load becomes lighter and the OCL pin detects I_D at ”Standby switch voltage” (V_{OCL} (stby)) = 40mV (typ) or less for longer than “Standby switch time” (Tstby) = 250ms (typ).



2) Burst mode control

In burst mode, the OCL pin detects ID, and every pulse is limited to “Standby threshold voltage” (VTH (stby)) = 60mV (typ) to control oscillation.

Vo is controlled linearly in normal mode. In burst mode, oscillation begins when the VF/B reaches “On-State voltage” (VF/B (stby start)) = 1.8V (typ) and stops when VF/B falls to “Under-Voltage lockou” (VF/B (stby stop)) = 0.8V (typ). This control causes voltage ripples and intermittent oscillation, reducing switching loss per unit time and thereby reducing standby power consumption.

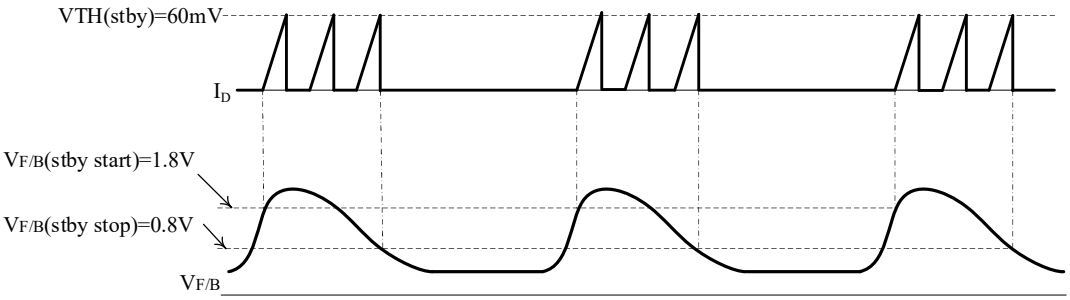
The following thresholds of VCC also change from normal mode:

○ “Under-Voltage lockout” and “Start-Up circuit on voltage” are lowered by 1V from normal mode.

“Under-Voltage lockout” : VCC (stop normal) = 8V (typ) → VCC (stop stby) = 7V (typ)

“Start-Up circuit on voltage” : VCC (stup on normal) = 9V (typ) → VCC (stup on stby) = 8V (typ)

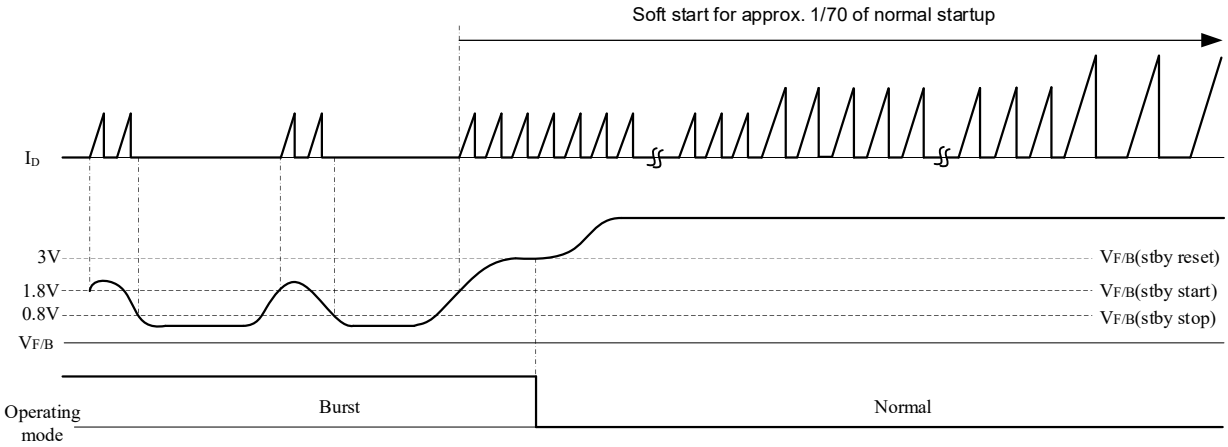
These allow down to the VCC setting in burst mode and further reduce power consumption



3) Switching from burst mode to normal mode

The IC switches automatically to normal mode when the load becomes heavier and VF/B rises and exceeds “Standby reset F/B voltage” (VF/B (stby reset)) = 3V (typ).

The thresholds changed at standby return to previous levels when the IC returns from burst mode to normal mode. At the same time, soft start activates for approximately 1/70 of the normal startup to prevent jitter and other problems during mode switching.

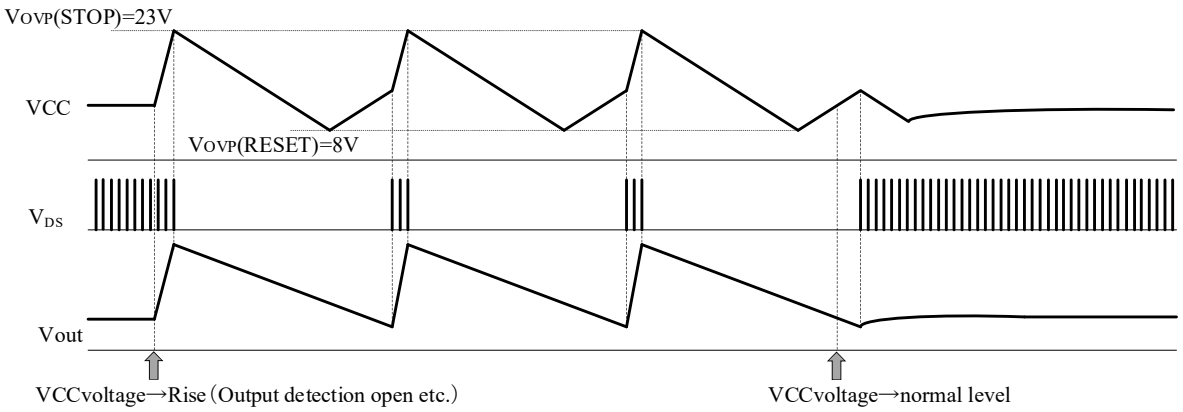


3.4 Protection functions

3.4.1 Vcc overvoltage protection (OVP) Auto recovery mode

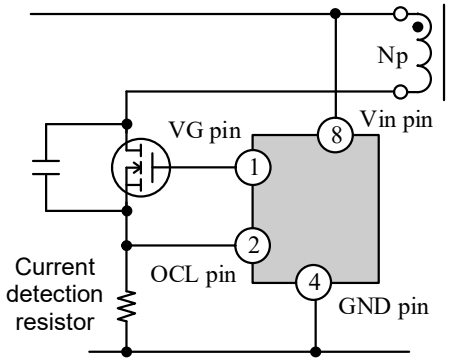
The IC incorporate an auto recovery mode overvoltage protection circuit (OVP).

VCC voltage smoothed with Nc winding voltage stops operating at over-voltage threshold V_{OVP} (STOP) = 23V (typ) and above. Indirectly overvoltage protection of secondary side output. Also, when the VCC voltage drops to over-voltage reset threshold V_{OVP} (RESET) = 8V (typ) or less after the operation stops, the startup circuit starts to operate and resumes operation when on-state voltage VCC (start) = 12V (typ) or above.

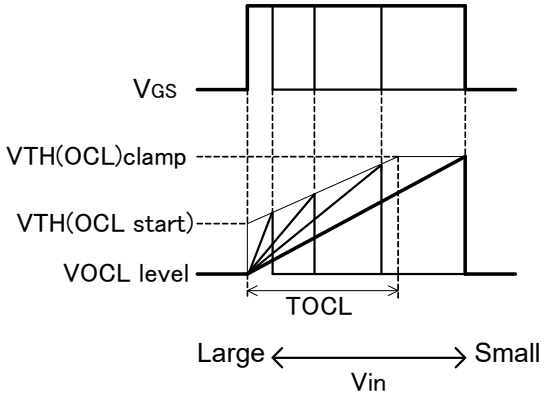


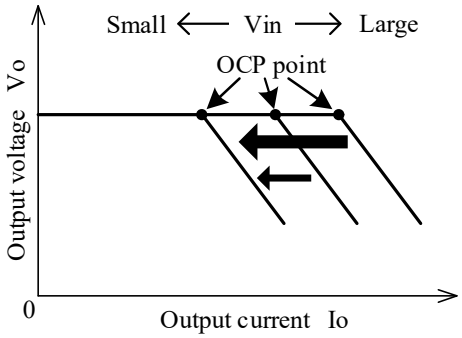
3.4.2 Overcurrent protection (OVP)

A current detection resistor is connected between the OCL pin and the GND pin to detect the source current of the main switching device. The main switching device current is limited by pulse-by-pulse operation using a threshold voltage that varies with the on-time.



This current limit protection function incorporates a function to correct dependence on input voltage : Vin. The function changes the OCL threshold on the IC from the ”Over current limit correction start voltage” (VTH (OCL start)) = 0.38V (typ) to “Over current limit correction clamp voltage” (VTH (OCL) clamp) = 0.54V (typ) linearly with the on-time. Since the slope (di/dt) of I_D of the main switching device is proportional to Vin, when Vin increases, the current reaches the OCL threshold with smaller a main switching device peak current : I_{DP}, and the drooping-point is corrected.

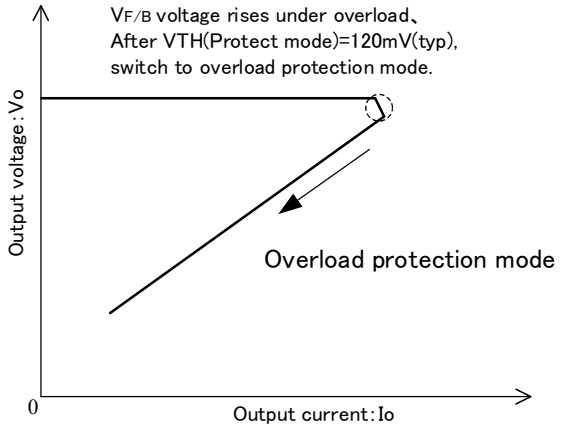


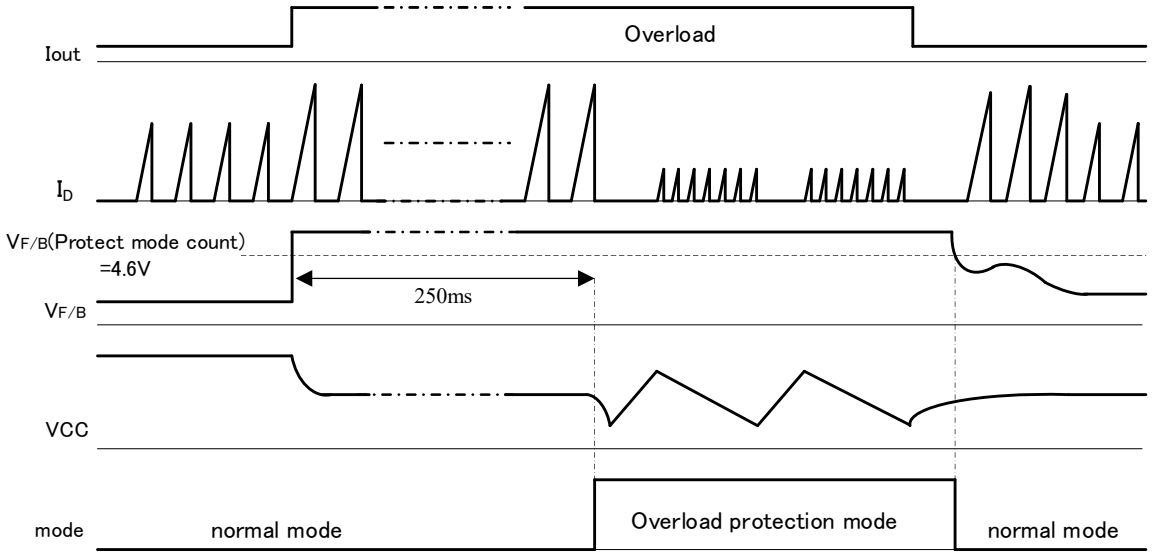


3.4.3 Overload protection (Auto recovery mode)

The overload protection function raises the $V_{F/B}$ voltage under overload. If the $V_{F/B}$ voltage is above the protect mode count start voltage "($V_{F/B}$(protect mode count) = 4.6V(typ))" voltage and continues the protect count mode time" (T(protect count mode) = 250ms(typ))", it will switch to overload protection mode.

The overload protection mode limits current when the overcurrent detection is changed from the overcurrent limit correction clamp voltage "(VTH(OCL)clamp = 0.54V (typ))", which is the threshold of normal operating mode, to the protected mode threshold voltage "(VTH (Protect mode) = 120mV (typ))". Also, turn off the bias assist function.





3.4.4 VCC-GND short circuit protection

If VCC and GND short-circuit, current flows continuously to the startup circuit, and heat builds up in the IC. A function reduces s “VCC current” (ICC) in the event of short circuits to prevent excessive heat buildup.

3.4.5 Leading edge blank (LEB)

The IC incorporate “Leading edge blanking time” (TLEB) = 300ns, which rejects trigger signals from ID detection circuit for a certain period of time after the main switching device is turned on to improve the noise margin.

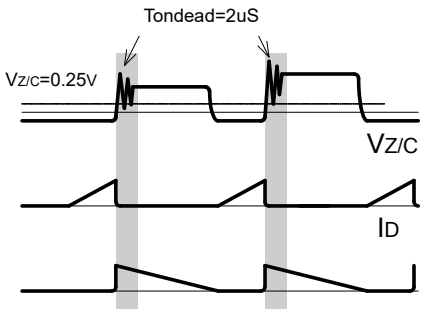
This function prevents false detection due to a gate drive current generated the moment the main switching device is turned on or to a current discharged from the resonating capacitor.

3.4.6 On-trigger malfunction prevention circuit (Tondead)

At startup or in the event of a load short circuit, Vo drops to levels significantly below the set voltage. Since the control coil voltage is proportional to Vo, it drops significantly as well. In this case, a false on-trigger timing may be detected due to the ringing voltage while the device is off. The device may be turned on before the current critical point.

To address this problem, the IC incorporate a circuit for preventing on-trigger malfunctions at startup or in the event of short circuits.

This function disables “On dead time (Tondead) = 2μs” after the main switching device in the IC is turned off. This prevents false detection due to the ringing voltage while the device is off.



3.4.7 Thermal shutdown (TSD) Auto recovery mode

Thermal shutdown (TSD) will stop oscillation when it becomes over temperature sense stop “OTS (H) = 150°C (typ)”. It will strike when you go down to over temperature sense Reset “OTS (L) = 110°C (typ)”.

Also, there is a hysteresis operation for temperature detection and it is an auto recovery mode.

4. Pin functions

4.1 Z/C pin

The Z/C pin detects the NC winding voltage and outputs a turn-on signal. The pin has the following functions:

1) Gate on-trigger
2) Prevention of false turn-on (Tondead)
3) Bottom skip

4.2 F/B pin

The F/B pin determines the on-time during constant voltage control. The pin has the following functions:

1) Determination of the on-time for the F/B pin voltage (gate off-trigger)
2) Switch to overload protection mode

4.3 GND pin

The GND pin is used as the ground reference of the IC.

4.4 OCL pin

The OCL pin uses a detection resistor to limit the primary current. The pin has the following functions:

1) Determination of the primary current peak during the four-step soft-start
2) Determination of the primary current peak during the auto-burst mode (auto-standby mode)
3) Determination of the maximum primary current peak (pulse-by-pulse)
4) Leading edge blank function

4.5 VG pin

The VG pin outputs a gate voltage and has the soft drive function.

4.6 VCC pin

The VCC pin is the IC power terminal and has the following functions:

1) UVLO
2) ON/OFF of the startup circuit
3) Bias assist
4) OVP
5) VCC-GND short circuit protection

4.7 Vin pin

The Vin pin is connected to the positive side of the input capacitor and is used to power on the IC.

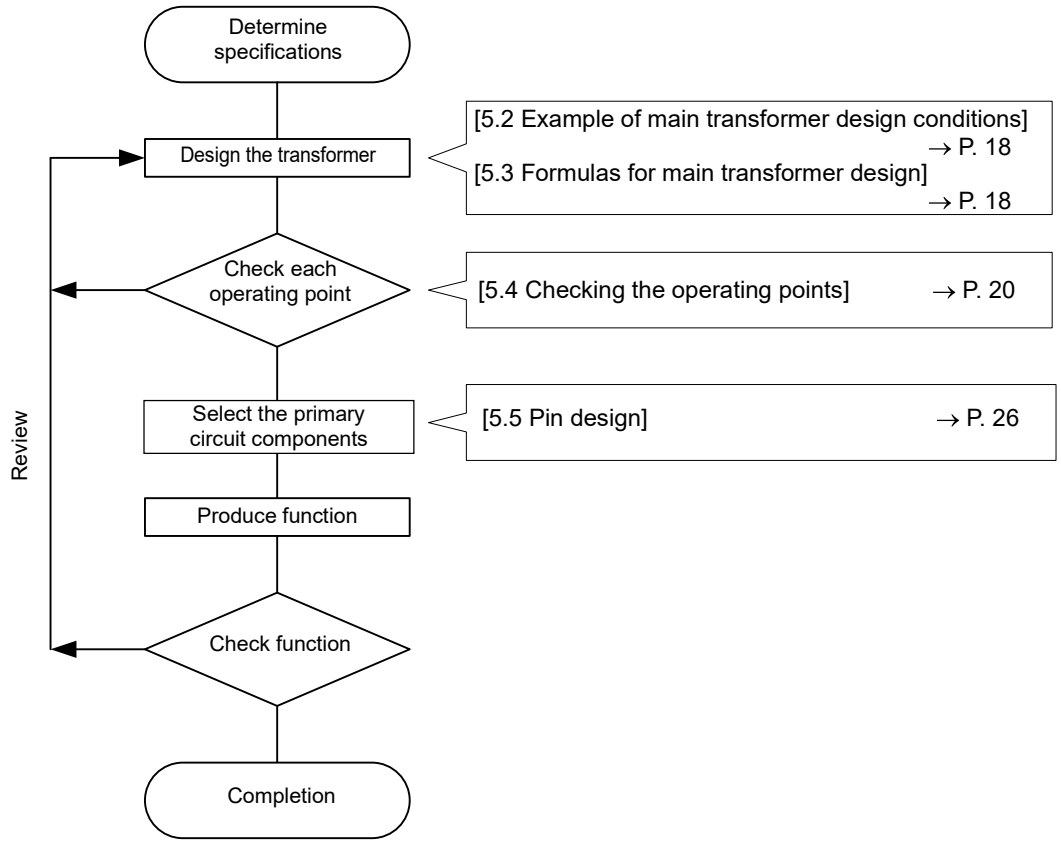
5. Design procedure

The design procedure presented in this section is intended to illustrate an example of electrical design procedure. Make sure insulation materials, insulation configuration, and structure meet the safety standards set forth by the relevant authorities. The following table shows the units for the parameters used in the formulas encountered in this section:

• List of units used in the formulas in this section

Description	Unit	Description	Unit
Voltage	V (volt)	Time	s (second)
Current	A (ampere)	Length	mm (millimeter)
Power	W (watt)	Area	mm^2 (square millimeter)
Capacitance	F (farad)	Current density	A/mm^2 (ampere per square millimeter)
Inductance	H (henry)	Magnetic flux density	mT (millitesla)
Resistance	Ω (ohm)	Number of turns	turn

5.1 Design flow chart



5.2 Example of main transformer design conditions

The values below are provided as guideline values only. Make the appropriate adjustments to suit specific load conditions.

Description	Symbol	Unit	Reference value
Input voltage range	V_{AC}	[V]	85–276
Efficiency	η	-	0.80–0.85
Minimum oscillation frequency	$f_{(min)}$	[kHz]	35–50
On duty ratio	D	-	0.4–0.6
Capacity of resonating capacitor	Cq	[pF]	100–3300
Control voltage	V_{NC}	[V]	15–20
Magnetic flux density variation	ΔB	[mT]	250–300
Winding current density	α	[A/mm^2]	4–6

* If the output capacity of the main switching device Coss is significant relative to the capacity setting of the resonating capacitor, Cq must be the capacity of the resonating capacitor plus Coss.

5.3 Formulas for main transformer design

1	Minimum DC input voltage	$V_{DC(\min)} = 1.2 \cdot V_{AC(\min)}$	[V]
2	Maximum DC input voltage	$V_{DC(\max)} = \sqrt{2} \cdot V_{AC(\max)}$	[V]
3	Maximum oscillation period	$T_{(\max)} = \dfrac{1}{f_{(\min)}}$	[s]
4	Maximum on-time	$t_{on(\max)1} = \dfrac{D}{f_{(\min)}}$	[s]
5	Maximum off-time	$t_{off(\max)} = \dfrac{N_{S1} \cdot V_{DC(\min)} \cdot t_{on(\max)1}}{Np \cdot (V_{O1} + V_{F1})} + tq$	[s]
6	Quasi-resonance-time	$tq = \pi \cdot \sqrt{Lp \cdot Cq}$	[s]
7	Maximum load power	$P_{O(\max)} = Vo \cdot I_{O(\max)}$	[W]
8	Maximum output power (reference value)	$P_L = 1.2 \cdot P_{O(\max)}$	[W]
9	Main switching device peak current	$I_{DP} = \dfrac{2 \cdot P_L}{\eta \cdot V_{DC(\min)} \cdot D}$	[A]

10	Primary winding inductance	$Lp = \frac{V_{DC(\min)} \cdot t_{on(\max)1}}{I_{DP}}$	[H]
11	Number of turns in primary winding	$Np = \frac{V_{DC(\min)} \cdot t_{on(\max)1} \cdot 10^9}{\Delta B \cdot Ae}$	[Turn]
12	Core gap	$\lg = \frac{4 \cdot \pi \cdot Ae \cdot Np^2 \cdot 10^{-10}}{Lp}$ * Ae : Effective sectional area of core [mm^2]	[mm]

* The gap Ig must be the center gap value.
* If the Ig is 1 mm or greater, review the transformer core size and oscillation frequency and consider a redesign.

13	Number of turns in control output winding	$N_{S1} = \frac{Np \cdot (V_{O1} + V_{F1}) \cdot (\frac{1}{f_{(\min)}} - t_{on(\max)1} - tq)}{V_{DC(\min)} \cdot t_{on(\max)1}}$	[Turn]
14	Number of turns in non-control output winding	$N_{S2} = N_{S1} \cdot \frac{V_{O2} + V_{F2}}{V_{O1} + V_{F1}}$	[Turn]
15	Number of turns in control winding	$Nc = N_{S1} \cdot \frac{V_{NC} + V_{FNC}}{V_{O1} + V_{F1}}$	[Turn]

* Symbols used in formulas 13 to 15

Control output winding: Output voltage 1	V_{O1}	Output of control output winding: Rectification diode forward voltage	V_{F1}
Non-control output winding: Output voltage 2	V_{O2}	Output of non-control output winding: Rectification diode forward voltage	V_{F2}
Control coil: Output voltage 1	V_{NC}	Output of control winding: Rectification diode forward voltage	V_{FNC}

* If the control winding voltage V_{NC} is not well regulated, set a lower value.

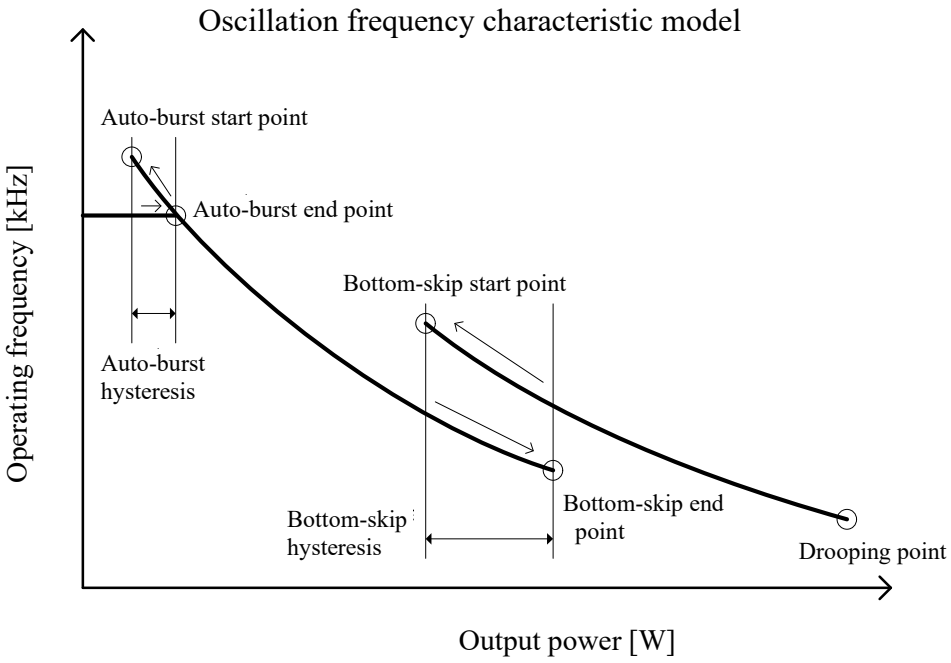
16	Primary winding sectional area	$A_{NP} = \frac{2 \cdot \sqrt{D} \cdot Po}{\alpha \cdot \sqrt{3} \cdot \eta \cdot V_{DC(\min)} \cdot t_{on(\max)1} \cdot f_{(\min)}}$	[mm^2]
17	Secondary winding sectional area	$A_{NS} = \frac{2 \cdot Io \cdot \sqrt{1 - D - (tq \cdot f_{(\min)})}}{\alpha \cdot \sqrt{3} \cdot (t_{off(\max)} - tq) \cdot f_{(\min)}}$	[mm^2]

* Shindengen recommend a wire diameter of 0.2mm or greater for the Nc winding to simplify calculations.

5.4 Checking the operating points

The IC have points of change at which the oscillation frequency changes according to the functions of the control IC.

Identifying each point helps predict the behavior of a prototype power supply. The following chart shows a model of operating frequency characteristics relative to output power. Knowing each operating point will provide approximate levels of the power, hysteresis width and droop point at these points of change.



The operating points to be calculated in this section are circled on the chart above.

- Bottom-skip start and end points
- Auto-burst start and end points
- Drooping-point

Obtain these points to check the following:

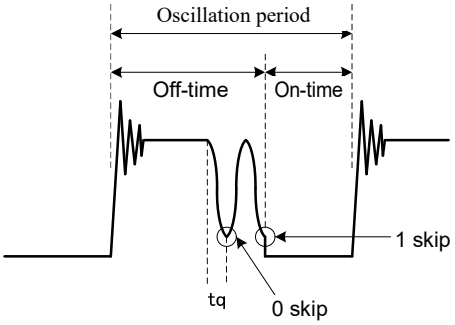
Is the standby operation properly performed in standby mode?

Is the bottom-skip hysteresis sufficient?

Is the drooping-point sufficiently greater than the output?

5.4.1 Variables in formulas

Description	Symbol	Unit
DC input voltage setting	V_{DC}	[V]
On-time under each condition	ton	[s]
Off-time under each condition	toff	[s]
Main switching device peak current under each condition	IDP	[A]
Output power under each condition	Po	[W]
Primary current detection resistance	R(ocl)	[Ω]
OCL pin auto-burst threshold voltage	Vburst	[V]
OCL pin current detection threshold voltage	Vth(ocl)	[V]



Switching waveform model

The diagram to the right shows switching waveform models, including numbers of bottoms to skip and tq. For other symbols, see Section 5.3 and the specification.

5.4.2 Formulas for obtaining bottom skip start power

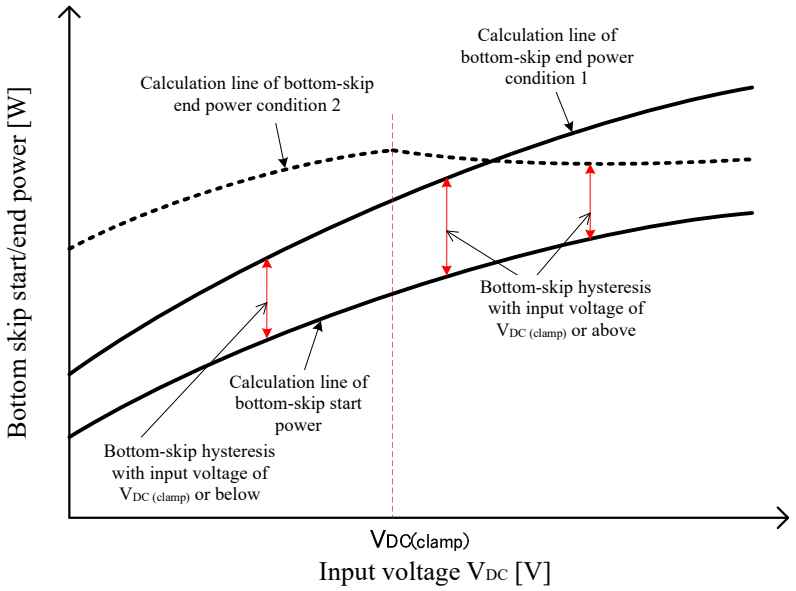
18	On-time	$ton = \frac{Np \cdot (T_{(\text{bottom\_skip\_start})} - tq) \cdot (V_{O1} + V_{F1})}{N_{S1} \cdot V_{DC} + Np \cdot (V_{O1} + V_{F1})}$	[s]
19	Off-time	$toff = T_{(\text{bottom\_skip\_start})} - ton$	[s]
20	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
21	Bottom-skip start power	$Po = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot T_{(\text{bottom\_skip\_start})}}$	[W]

If the bottom-skip start power obtained by the formulas above is greater than the bottom-skip end power obtained in Section 5.4.3, the hysteresis is insufficient; redesign the transformer.

5.4.3 Bottom-skip end power

The bottom-skip function ends when either Condition 1 or Condition 2 is met. The bottom-skip end power will be the “bottom-skip end power 1 of the formula 25 of Condition 1” or the “bottom-skip end power 2 of the formula 30 or the bottom-skip end power 3 of the formula 34 of Condition 2,” whichever is smaller. (Depending on the input voltage you want to calculate, compare either the bottom-skip end power 2 or 3 of Condition 2 to bottom-skip end power 1.)

The chart on the next page shows model curves of bottom-skip start and end power levels relative to input voltage.



[Condition 1] The operating frequency fulfills T (bottom_skip_stop).

22	On-time	$ton = \frac{Np \cdot (T_{(\text{bottom\_skip\_stop})} - tq) \cdot (V_{O1} + V_{F1})}{N_{S1} \cdot V_{DC} + Np \cdot (V_{O1} + V_{F1})}$	[s]
23	Of-time	$toff = T_{(\text{bottom\_skip\_stop})} + 2tq - ton$	[s]
24	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
25	Bottom skip end power 1	$Po = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2Lp \cdot (T_{(\text{bottom\_skip\_stop})} + 2tq)}$	[W]

[Condition 2] The OCL pin voltage reaches the current detection threshold voltage in bottom-skip mode.

Under this condition, Vth (ocl) varies with input voltage. First, calculate the input voltage $V_{DC\ (clamp)}$ at the point of change in Vth (ocl). If V_{DC} does not exceed $V_{DC\ (clamp)}$, apply the formulas in next page 1). If V_{DC} exceeds $V_{DC\ (clamp)}$, apply the formulas in 2).

The $V_{DC\ (clamp)}$ (Input voltage at the point of change in Vth (ocl)) is obtained with the following formula.

26	Input voltage at the point of change in Vth (ocl)	$V_{DC(clamp)} = \frac{Lp \cdot Vth_{(OCL)clamp}}{TOCL \cdot R_{(OCL)}}$	[V]

1) $V_{DC} < V_{DC\ (clamp)}$

27	On-time	$ton = \frac{Lp \cdot Vth_{(OCL)clamp}}{V_{DC} \cdot R_{(OCL)}}$	[s]
28	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + 3tq$	[s]
29	Main switching device peak current	$I_{DP} = \frac{Vth_{(OCL)clamp}}{R_{(OCL)}}$	[A]
30	Bottom-skip end power 2	$Po = \frac{V_{DC} \cdot Vth_{(OCL)clamp} \cdot \eta \cdot ton}{2 \cdot R_{(OCL)} \cdot (ton + toff)}$	[W]

2) $V_{DC} > V_{DC\ (clamp)}$

31	On-time	$ton = \frac{Vth_{(OCLstart)}}{\frac{V_{DC} \cdot R_{(OCL)}}{Lp} - \frac{(Vth_{(OCL)clamp} - Vth_{(OCLstart)})}{T_{(ocl)}}}$	[s]
32	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + 3tq$	[s]
33	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
34	Bottom-skip end power 3	$Po = \frac{V_{DC}{}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot (ton + toff)}$	[W]

5.4.4 Auto-burst start/end power

For Vburst in the formulas, substitute the VOCL (stby) or VTH (stby) indicated under “Auto standby modde” of “Electric/thermal characteristics” in the specification.

To obtain auto-burst start power, substitute VOCL (stby) = 40mV in place of Vburst.

To obtain the auto-burst end power, substitute VTH (stby) = 60mV in place of Vburst.

35	On-time	$ton = \frac{Lp \cdot Vburst}{V_{DC} \cdot R_{(OCL)}}$	[s]
36	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + 3tq$	[s]
37	Main switching device peak current	$I_{DP} = \frac{Vburst}{R_{(OCL)}}$	[A]
38	Auto burst start/end power	$Po = \frac{V_{DC} \cdot Vburst \cdot \eta \cdot ton}{2 \cdot R_{(OCL)} \cdot (ton + toff)}$	[W]

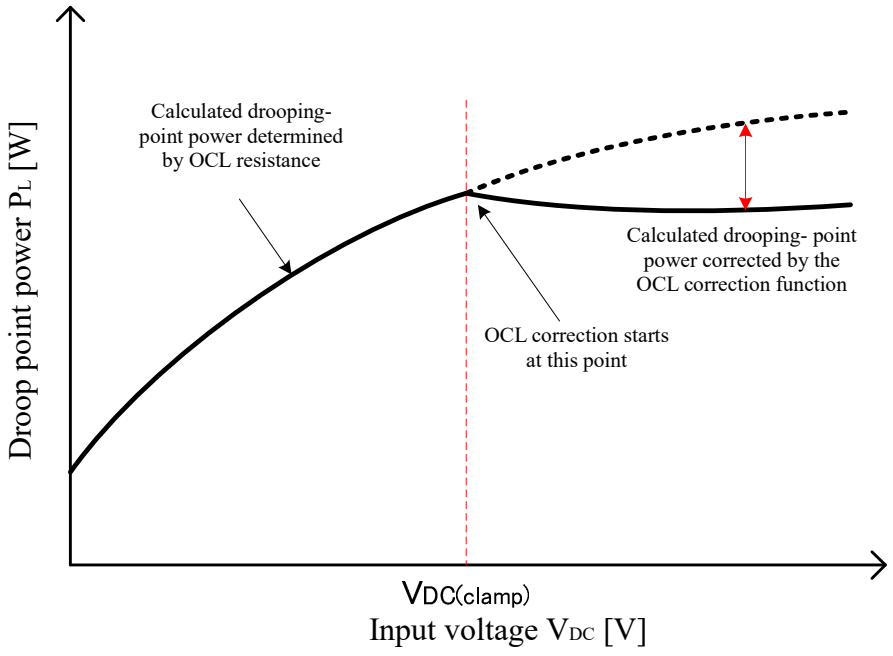
5.4.5 Drooping-point power

Vth (ocl) varies with input voltage. First, calculate the input voltage VDC (clamp) at the point of change in Vth (ocl). If VDC does not exceed VDC (clamp), apply the formulas in next page 1). If VDC exceeds VDC (clamp), apply the formulas in next page 2).

Just as in Section 5.4.3, use the following formula to obtain the input voltage at the point of change in Vth (ocl).

26	Input voltage at the point of change in Vth (ocl)	$V_{DC(clamp)} = \frac{Lp \cdot Vth_{(OCL)clamp}}{TOCL \cdot R_{(OCL)}}$	[V]

The chart below shows a model curve of the relationship between input voltage and droop point power.



1) $V_{DC} < V_{DC\ (clamp)}$

39	On-time	$ton = \frac{Lp \cdot Vth_{(OCL)clamp}}{V_{DC} \cdot R_{(OCL)}}$	[s]
40	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np(V_{O1} + V_{F1})} + tq$	[s]
41	Main switching device peak current	$I_{DP} = \frac{Vth_{(OCL)clamp}}{R_{(OCL)}}$	[A]
42	Drooping-point power	$P_L = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot (ton + toff)}$	[W]

2) $V_{DC} > V_{DC\ (clamp)}$

43	On-time	$ton = \frac{Vth_{(OCLstart)}}{\frac{V_{DC} \cdot R_{(OCL)}}{Lp} - \frac{(Vth_{(OCL)clamp} - Vth_{(OCLstart)})}{TOCL}}$	[s]
44	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + tq$	[s]
45	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
46	Drooping-point power	$P_L = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot (ton + toff)}$	[W]
47	Vth (ocl) at drooping-point	$Vth_{(ocl)} = \frac{(Vth_{(OCL)clamp} - Vth_{(OCLstart)})}{TOCL} \cdot ton + Vth_{(OCLstart)}$	[V]

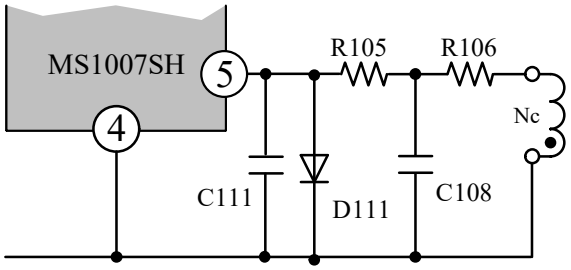
The results of calculations for the operating points above are provided as guidelines. They may differ from actual power supply characteristics for various reasons, including power supply efficiency, filter circuit, and control IC signal delays.

5.5 Pin design

5.5.1 Design procedure for the Z/C pin (Pin 5)

(1) Basic circuit

This is the simplest circuit configuration for designs requiring only normal mode. Since auto burst-mode is available, it is the easiest design for a power supply featuring standby mode.

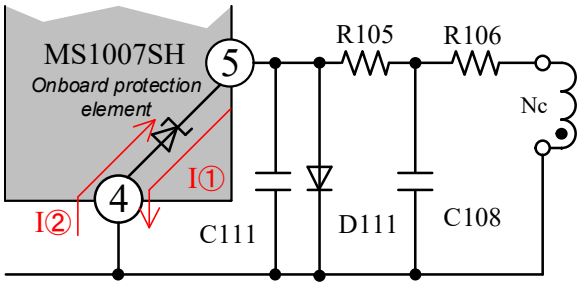


(2) Setting components

1) R105 + R106

The absolute maximum rating of the Z/C pin is ±5 mA. A zener diode is mounted for protection between the Z/C pin (Pin 5) and the GND pin (Pin 4). This diode determines the absolute maximum current rating. Set resistance so that the current does not exceed this level.

The diagram to the right shows a model circuit, which is a basic circuit with an onboard protection element (zener diode) added. I① and I② represent currents flowing to this onboard protection element. The current I① flows when the Nc winding output is a positive voltage. I② flows when the Nc winding output is a negative voltage.



I① and I② must not exceed the absolute maximum rating. In ordinary designs, set resistance so that these currents do not exceed 80% of the absolute maximum rating (± 4 mA).

The following table gives formulas for calculating the resistance R105 + R106:

48	Resistance assuming a positive voltage for Nc winding	$R105 + R106 \geq \dfrac{\dfrac{Nc \cdot (V_{O1} + V_{F1})}{N_{S1}} - VCL(H)}{I_{①}}$	[Ω]
49	Resistance assuming a negative voltage for Nc winding	$R105 + R106 \geq \dfrac{\dfrac{Nc \cdot V_{DC(\max)}}{Np} - VCL(L)}{-I_{②}}$	[Ω]

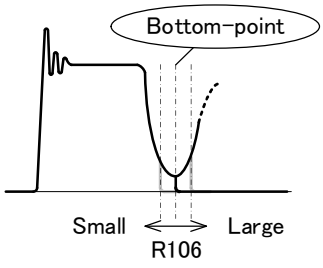
VCL (H) and VCL (L) are the clamping voltages of the onboard protection element, a protective zener diode. The specification gives these values.

If the basic circuit configuration shown in Section 1.5 is used, I① flows to the D111. In this case, formula 48 may be disregarded.

2) R106 and C108

These components set up the quasi-resonance period tq.

Adjust to the quasi-resonance bottoms while monitoring actual waveforms.



Symbol	Initial design value
C108	47 pF
R106	220Ω or greater

The maximum voltage applied to both ends of C108 is calculated as shown in the formula 50. Determine the withstand voltage of C108 by referring to the calculated value.

50	Maximum voltage applied to both ends of C108	$V_{C108} = (V_{O1} + V_{F1}) \frac{Nc}{N_{S1}} + V_{DC(max)} \frac{Nc}{Np}$	[V]

3) C111

C111 is a noise countermeasure part. It uses a high frequency characteristic condenser and is about 33pF. For large capacity, it becomes difficult to adjust the valley point. Also, the voltage is the same as the value (C108) calculated by the 50 formula.

4) D111

C111 is an abnormal countermeasure part. We recommend adding. Please select the small fast recovery diode (FRD) of reverse recovery time (Trr).

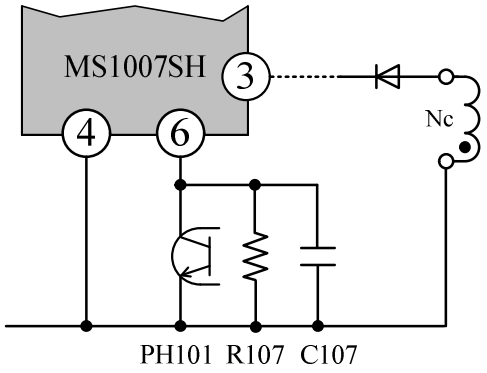
As described in section 3.2.1, the on-trigger circuit detects the Z/C pin voltage when it reaches $V_{Z/C}$ = 0.25V (typ). Thus, the diode should not reduce the voltage below $V_{Z/C}$. Make sure the diode has adequate VF to secure $V_{Z/C}$.

5.5.2 Design procedure for F/B pin (6pin)

(1) Basic circuit

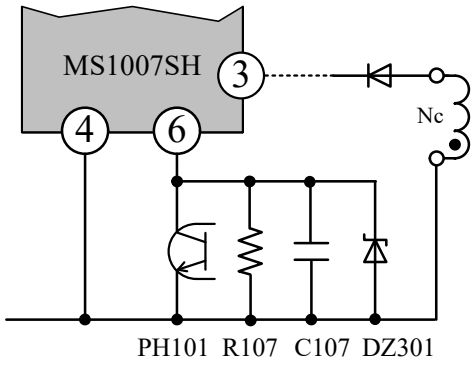
The diagram to the right shows the basic circuit. PH101 is a photocoupler for constant voltage control. R107 and C107 are noise reduction components.

C107 has a capacitance between 470pF and 2200pF. Set the initial design value to 1000pF. R107 is set between 39kΩ and 47kΩ. Normally, it should be set to 47kΩ. If the resistance falls below 39kΩ, the timer latch function may be disabled.



(2) Circuit Protection

PH101 may exhibit insulation breakdown during a short circuit test. If so, protect the circuit using a zener diode, as shown to the right. A zener diode (ZD301) for 10V or greater should have negligible effect on IC functions for normal use.

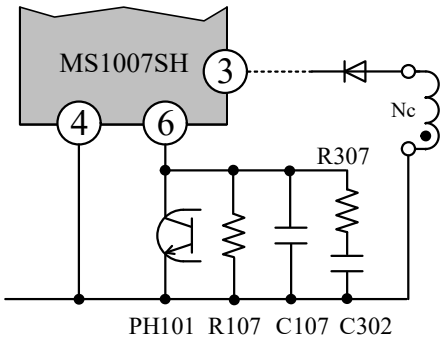


(3) Phase compensation of F/B pin

C107 is used not just to reduce noise, but to adjust feedback response. However, in a large-capacity or multi-output power supply, phase compensation by the secondary control circuit may be inadequate.

If so, add a circuit between the F/B pin and the GND pin, as shown to the right. Doing so can resolve various issues, including hunting.

Refer to the following table to determine constants.



Symbol	Initial design value
R307	4.7 kΩ
C302	0.1 μF

(4) Additional circuit to F/B pin

When adding a circuit to the power supply circuit due to load setting conditions or for other reasons, be careful to avoid disabling the protect mode function. Disabling the protect mode will affect power supply performance.

5.5.3 Design of OCL pin (2pin)

(1) Basic circuit

The diagram to the right shows the basic circuit.

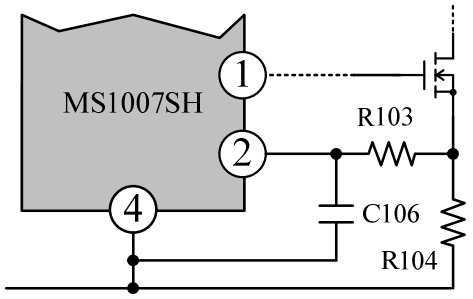
The circuit consists of R104 for primary current detection and a filter circuit comprising R103 and C106.

R104: Resistance required in Section 5.4

C106: Initial design value of 220pF
Design values from 220pF to 3300pF

R103: Initial design value of 100Ω
Design values from 100Ω to 470Ω

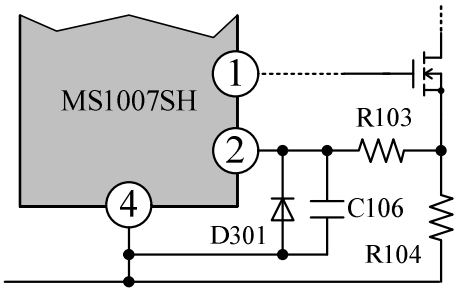
Increase the constants if switching noise is significant and may lead to malfunctions.



(2) Protection for large output power

If switching noise is significant for instance, because output power is large a high negative voltage may be applied to the OCL pin. Since the IC are single power supply ICs, a negative voltage may damage the IC or cause malfunctions.

The following diagram shows a circuit that incorporates a feature to protect the OCL pin against negative voltages. The added diode D301 should have small V_F (a Schottky barrier diode is recommended) and should be connected as close as possible to the pin.

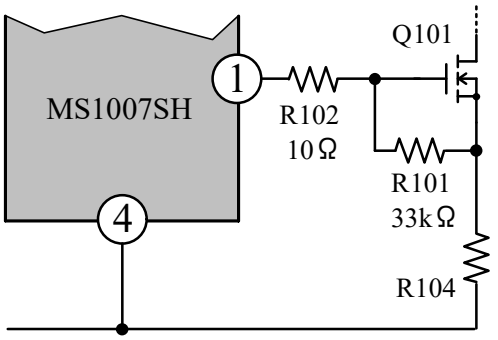


5.5.4 Design of VG pin (1pin)

(1) Basic circuit

The VG pin outputs switching signals. It can be used when the main switching device is a voltage-driven element.

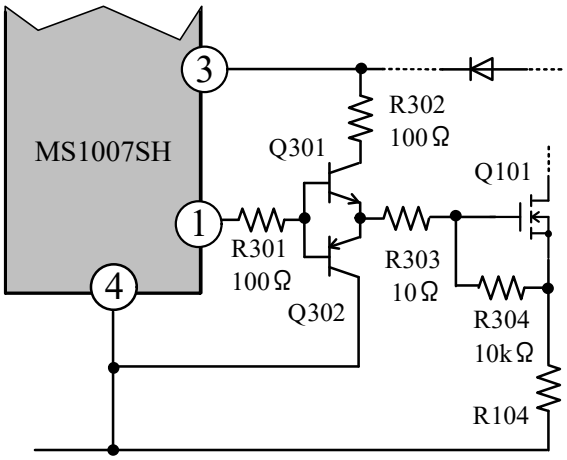
The diagram to the right shows the basic circuit configuration. The initial design values should be 10Ω for the gate resistor R102 and 33kΩ for the resistor R101 between the gate and the source.



(2) Circuit requiring a drive circuit

The main switching device driving performance of the IC series is specified under "Soft drive" of "Electric/thermal characteristics" in the specification. A circuit for enhancing the driving performance is required between the V_G pin and the main switching device as shown to the right if the main switching device cannot be driven directly by the V_G pin in the basic circuit (1).

Refer to the diagram to the right to determine constants.



Use the gate total charge quantity Qg of the main switching device as a guide for determining whether a driving circuit is required.

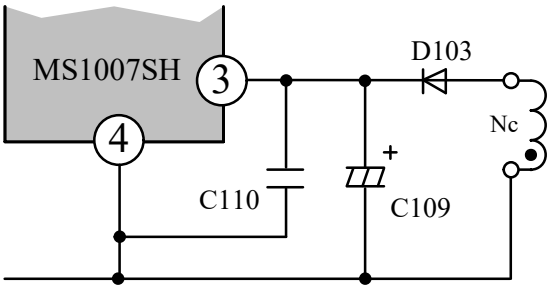
Qg of main switching device > 21 nC to 25 nC	Driving circuit required
Qg of main switching device < 21 nC	No driving circuit required

5.5.5 Design of VCC pin (3pin)

(1) Basic circuit

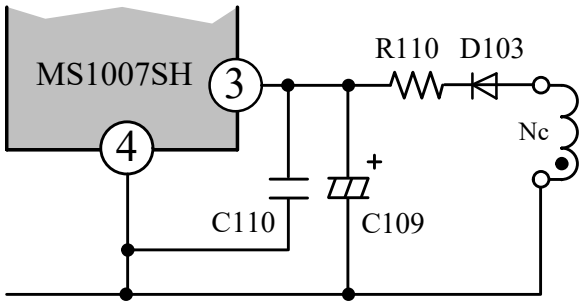
The diagram to the right is the basic circuit. The circuit consists of D103 and C109 for rectifying the Nc winding output and C110 for noise reduction between VCC and GND.

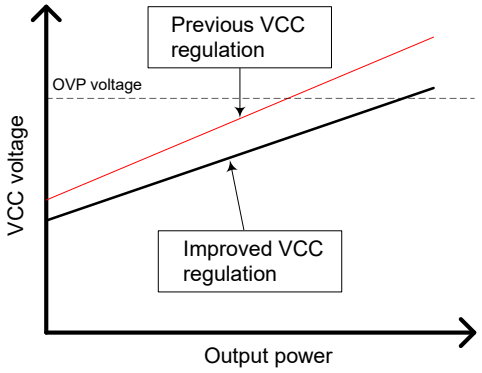
For C110, use a capacitor with good frequency characteristics. Design around 0.22μF.



(2) Measure (1) against poorly regulated VCC

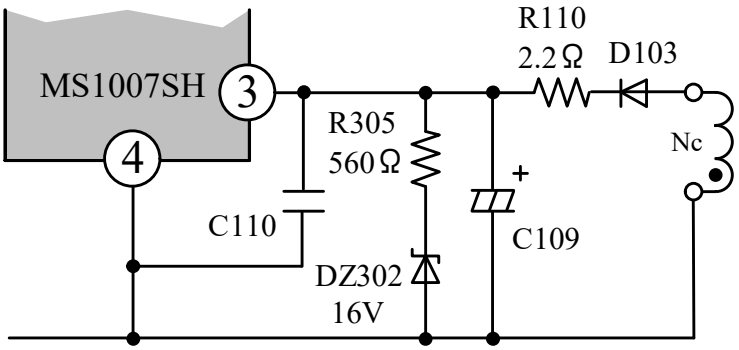
If the VCC is not well regulated due to design conditions, such as the load specification, add R110 as shown below to the left. This is generally the most cost-effective way to improve regulation. The chart to the right shows model lines of VCC regulation relative to output power. The red line represents VCC regulation with the basic circuit (1). The measure adjusts behavior to the black line.





(3) Measure (2) against poorly regulated VCC

The diagram below shows a circuit that improves regulation more effectively than measure (2).

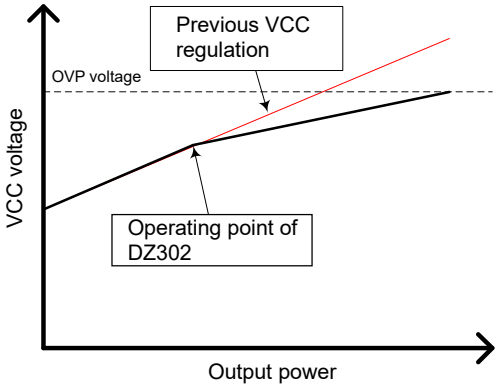


Symbol	Initial design value	Recommended value
R305	560 Ω	220 Ω～1 kΩ
DZ302	16 V	15 V～18 V

* Keep in mind potential losses associated with R305.

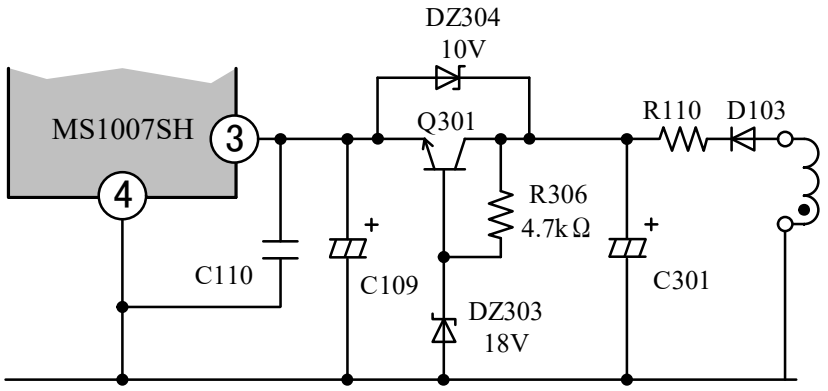
This measure will improve the regulation (represented by the red line) and move it to the bold line on the chart to the right. The voltage setting of DZ302 is the operating point of DZ302, as shown to the right.

This circuit incorporating this measure is the most effective circuit available when using super standby mode. No losses occur in super standby mode.



(4) Measure (3) against poorly regulated VCC

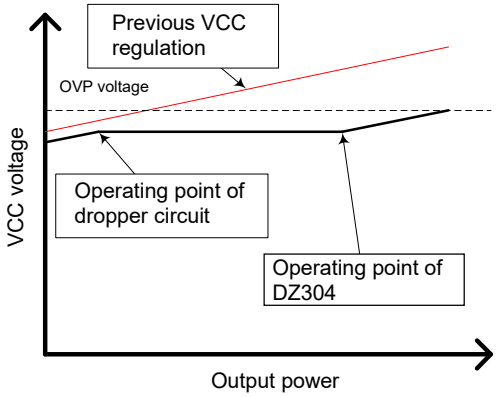
If the measures described in Section (2) and (3) above do not work, use a dropper circuit as shown below to stabilize VCC. Use the constants given below as guidelines.



When selecting DZ303, note the withstand voltage between Q301 and EB.
If the withstand voltage between Q301 and EB is 5V, select 18V or greater.
If the withstand voltage between Q301 and EB is 7V, select 16V～18V or greater.

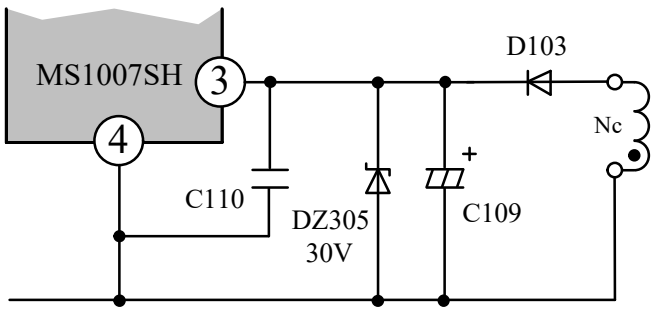
This measure stabilizes the VCC to the zener voltage of DZ303 plus V_{BE} of Q301. Unless DZ304 is added as shown in the diagram above, OVP of the VCC pin cannot be used. Set the zener voltage of DZ304 so that the OVP functions properly.

The chart to the right shows a VCC regulation model after implementing the measures above. Activating the dropper circuit stabilizes the voltage. When DZ304 activates, the voltage becomes the OVP voltage.



(5) Circuit protection

The VCC pin may break down during a short circuit test. If so, protect the circuit using a zener diode (DZ305), as shown to the right. A zener diode for 30V or greater should have negligible effect on IC functions for normal use.



5.5.6 Setting resonating capacitor

The capacitance set for the resonating capacitor should be between 47pF and 2200pF for real-world applications. No other restrictions apply.

(1) Conditions under which a relatively large capacitance is selected

- The quasi-resonance bottom is close to 0V because, for example, input voltage is low and the main switching device loss is expected to be very small.
- The conducted emissions are high.
- The surge voltage is large relative to the withstand voltage of the main switching device, and there is no margin.

(2) Conditions under which a relatively small capacitance is selected

- The main switching device generates significant heat.
- Standby power must be minimized.

The following table lists the effects of changes in the capacitance of the resonating capacitor on power supply performance.

Item	Reduce capacitance.	⇔	Increase capacitance.
Main switching device peak voltage	Rise	⇔	Fall
Drooping- point power	Increase	⇔	Decrease
Heat buildup in the main switching device	Decrease	⇔	Increase
Main switching device current immediately after powering on	Decrease	⇔	Increase
Main switching peak current under the same output power conditions	Decrease	⇔	Increase
Regulation of Vo	Decline	⇔	Improve
Regulation of VCC	Decline	⇔	Improve
Power supply efficiency	Improve	⇔	Decline
Noise	Rising tendency	⇔	Declining tendency

In efforts to optimize power supply performance, changes in the capacitance of the resonating capacitor often involve trade-offs. Carefully examine the advantages and disadvantages of the change when determining the constants. It may be possible to improve the trade-offs by redesigning the transformer. Consider redesigning the transformer to optimize power supply performance.

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