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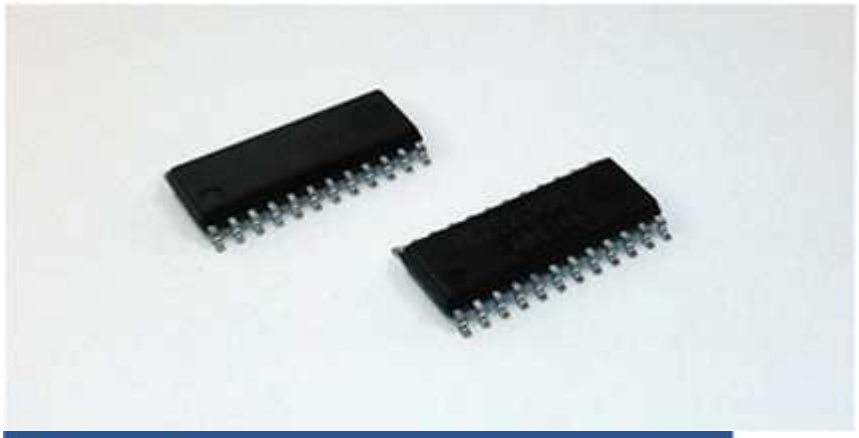
新電元

HV startup
Critical conduction Mode PFC controller
High performance LLC controller

All in one Green combo IC

MCZ5209SN



Smart-Resoic®

Application Manual

Ver. 0.1 b (en)

新電元工業株式會社

Shindengen Electric Manufacturing Co., Ltd.

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Table of contents

1 General description

MCZ5209SN is a LLC resonant controller with integrated CRM(Critical conduction mode / Transition mode / Boundary conduction mode) PFC controller and loss-less startup high voltage switch in one chip. Active standby fucnction and burst mode operation improves light load efficiency.
600V withstandng high side direct gate driver and optimised protection assures robust compact resonant converter design by minimum component counts in high power applications like :

- LBP and OA equipment PSU
- AC adapters
- Flat panel TV/display PSU
- Industrial equipment PSU
- High power LED driver
- Audio amplifier PSU

1.1 Features

[common features]

1. Integrated PFC controller and LLC controller in SOP24(narrow) package
2. HV self-bias switch eliminates external startup resistor consumption or additional bias converter
3. Frequency / interval adjustable burst function
4. Active stdby function improves light load efficiency
5. Latched or non-latched protection selectable
6. TSD(Thermal shutdown) protects from heavy hazard of IC in abnormal condition
7. High IC supply withstanding (35V)

[PFC section]

1. Critical conduction mode operation
2. Bottom skipping operation minimizes turn-on loss
3. Current sensing resistor loss is small by low sensing threshold voltage (0.5V)
4. Loop open protection / dynamic OVP

[LLC section]

1. Highly reliable 600V gate driver
2. Stabilized gate drive VDD
3. Two mode OCP
   OCP1 : fast shutdown of gate pulse for load short condition
   OCP2 : slow frequency sweep protection for OLP
4. Capasitive mode protection
5. Brown Out protection
6. Safe startup function

1.2 Block diagram

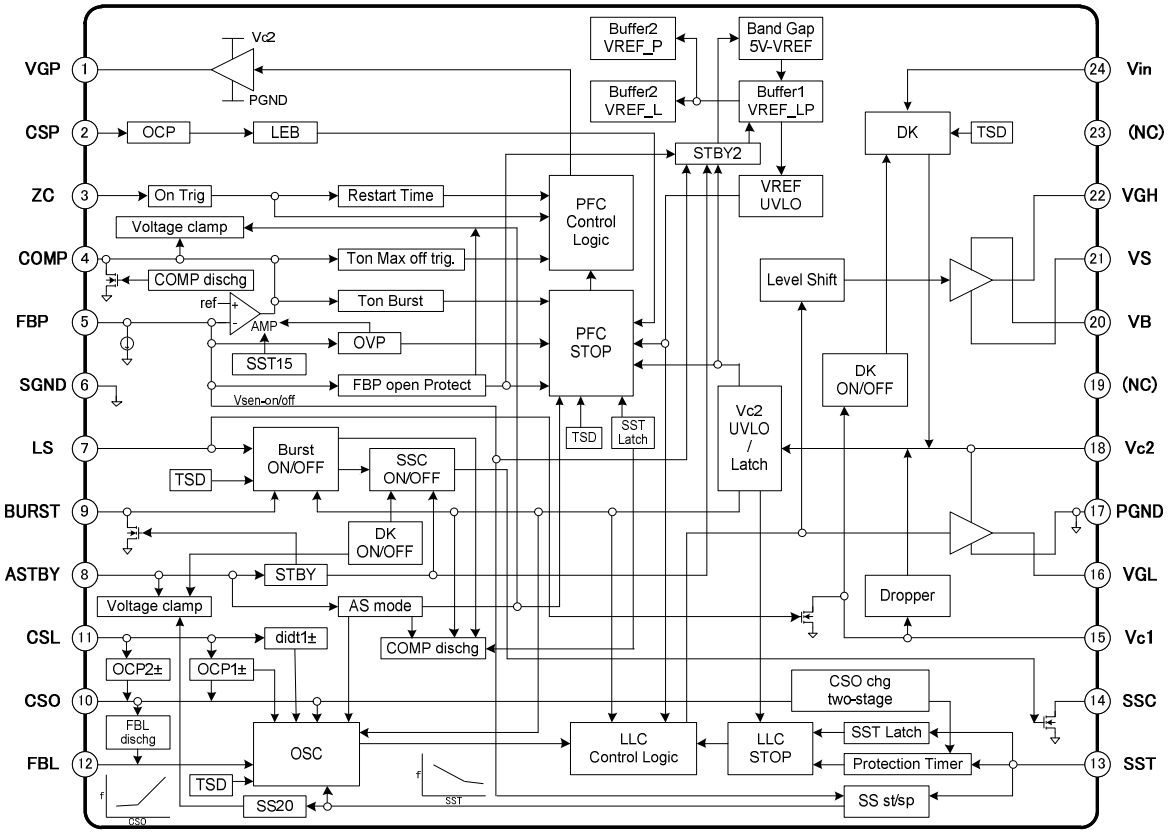


Fig.1 . MCZ5209SN internal block diagram

1.3 Pin assignment

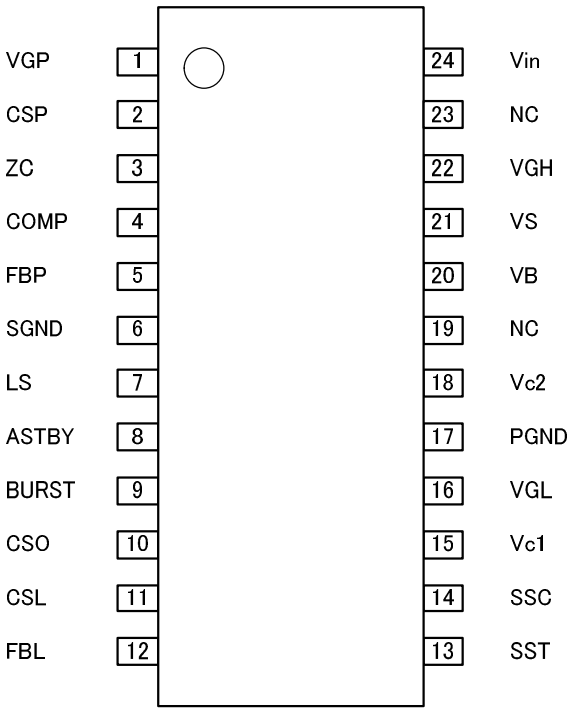


Fig.2 . MCZ5209SN pin assignment

1.4 Pin description

terminal	symbol	function
1	VGP	Gate drive output (PFC)
2	CSP	Current Sensing input (PFC) Protection threshold is 0.5V with LEB time of 200nsec
3	ZC	Zero Current detection signal input (PFC) Boost inductor sensing winding voltage is applied
4	COMP	error amp output for phase COMPensation(PFC) Connected to R/C filter
5	FBP	Feed Back input (PFC) : 3.0V threshold for PFC output, +8% for PFC dynamic OVP and 2.2V (0.2V hysterisis) for LLC brown-out
6	SGND	Signal Ground (PFC/LLC) Should be connected to PGND directly
7	LS	Line Sensing input (ALL) Usually used for AC input line sensing
8	ASTBY	Active Stdby / Burst mode selection terminal (ALL) IC operation mode is switched according to terminal voltage level
9	BURST	BURST interval adjusting (ALL) : Hi-Lo = LLC disabled, Lo-Hi = LLC enabled. 2.0V threshold with 0.2V hysterisis
10	CSO	Current Sense comparator Output (LLC) : connected to timing capacitor to adjust frequency limit protection response.
11	CSL	Resonant Current Sensing input (LLC) Used for fast OCP, slow OLP and capacitive mode protection.
12	FBL	Feed Back input (LLC) : used for fmin/fmax/fss/Dead Time adusting Connected to feedback opto coupler.
13	SST	Soft Start timing capacitor for normal mode connecting terminal. (LLC) Also used to adjust protection timer timing.
14	SSC	Soft Start timing capacitor for burst mode connecting terminal (LLC)
15	Vc1	Main IC supply input (ALL) : generally bias winding output DC voltage or external dc voltage is connected.
16	VGL	Gate drive output for Low side MOSFET (LLC)
17	PGND	Power Ground (PFC/LLC)
18	Vc2	Internal 12V regulator output for gate driver voltage source use (ALL)
19	NC	No connection (internally floating)
20	VB	Boot strapped voltage input for high side gate driver (LLC)
21	VS	LLC bridge point connecting terminal (LLC) Connected to source terminal of high side MOSFET
22	VGH	Gate drive output for High side MOSFET (LLC)
23	NC	No connection (internally floating)
24	Vin	HV startup switch input (ALL) High voltage input terminal for self bias

2 Functional description

- Ellectrical charactiristics values are described in TYP. condition.

2.1 introduction

2.1.1 Functional section

MCZ5209SN consists of four functional part as follows.
Functional description is described in section 2.2, component value selection is in section 2.3.

- **Supply section**
  Self bias and IC supply part . Refer to section 2.2.
- **PFC control section**
  PFC operation control and protections. Refer to section 2.3.
- **LLC control section**
  LLC operation control and protections . Refer to section 2.4
- **common control section**
  Refer to section 2.5.

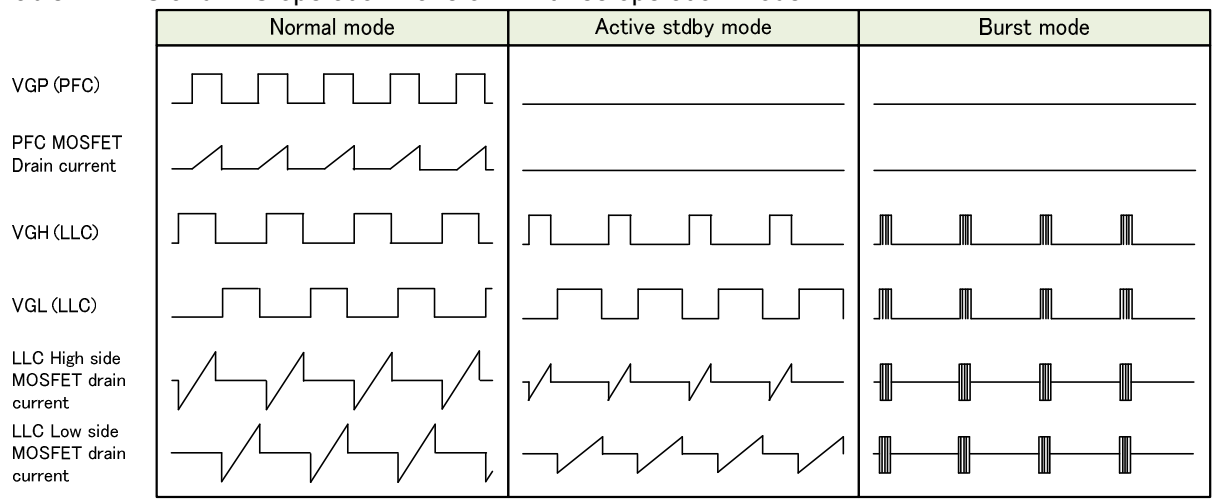
2.1.2 IC operation mode

MCZ5209SN has three operation modes.
PFC and LLC operation status is described in Table 1 and typycal operating waveform is shown in Table 2.
Operation mode switching timing detail is described in section 2.5.2.
IC operation mode is switched according to ASTBY terminal voltage level.
Normal mode operation is presupposed hereafter unless otherwise described.

Table 1. PFC and LLC operation status in tree operation mode

	Normal mode	Active stdby mode	Burst mode
PFC	Enabled	Disabled	Disabled
LLC symmetry	Symmetric	Asymmetric	Asymmetric
LLC operation	Continuous	Continuous	Burst mode

Table 2. PFC and LLC operation waveform in three operation mode



* LLC works asymmetrically in Burst mode.

2.2 Supply

2.2.1 IC supplies (HV startup self bias and internal Vc2 dropper)

MCZ5209SN has an internal high voltage startup switch. With this function, external bias converter can be eliminated and total highly efficient PSU is simplified.

Fig.3 shows the startup current flow. Internal high voltage switch sources constant charging current to Vc2 capacitor C237.

Vc2 Charging current is varied according to Vc2 terminal voltage : Idk(on)1=2.8mA at Vc2=1V and Idk(on)2=28.0mA at Vc2=4V.

When Vc2 terminal voltage exceeds 10V and PFC/LLC enabling condition is satisfied as described hereinafter, each converter enters into normal operation.

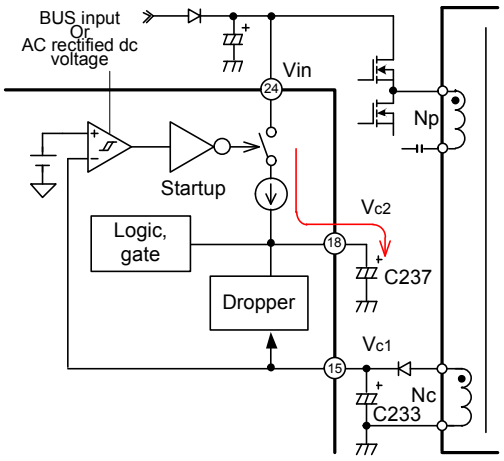


Fig..3 High voltage startup switch

In startup period Vc2 is charged until Vc2 terminal voltage reaches to 13.3V as long as Vc1 terminal voltage is less than Vc1(dkoff) of 12.6V. Vc1 voltage increases by self-biased dc voltage charging from bias winding after LLC starts operating.High voltage switch cut offs when Vc1 terminal voltage exceeds Vc1(dkoff) of 12.6V and IC supply becomes only from self-bias winding dc voltage.After high voltage startup switch cut offed, Vc2 terminal voltage is clamped to Vc2(dkoff) of 12.0V.

When Vc1 terminal voltage decreased to Vc1(dkon) of 8.0V, high voltage startup switch turn ons again. IC stops operation when Vc2 terminal voltage decreased to Vc2(SP) of 8.0V.

Vc1 and Vc2 capacitor should be enough value to keep normal startup/shutdown sequence, generally 100u – 470uF (these values influence to burst interval and input power consumption also).

If C233 or C237 position is distant from IC terminal, place filtering MLCC of 0.1u-1uF close to IC to prevent malfunction.

Table .3 IC supply operation threshold and characteristics

parameter	synbol	condition	Typ. spec
HV bias switch sourcing current 1	Idk(on)1	Vin=100V,Vc2=1.0V	2.8 mA
HV bias switch sourcing current 2	Idk(on)2	Vin=100V,Vc2=4.0V	28.0 mA
Vc2 voltage at HV bias switch = on	Vc2(dkon)	Vin=100V	13.3 V
Vc2 voltage at HV bias switch = off	Vc2(dkoff)	Vc1=16V	12.0 V
Vc1 voltage of HV bias disable	Vc1(dkoff)	Vin=100V	12.6 V
Vc1 voltage of HV bias enable	Vc1(dkon)	Vin=100V	8.0 V
Vc2 UVLO threshold (on)	Vc2(st)		10.0 V
Vc2 UVLO threshold (off)	Vc2(sp)		8.0 V

2.3 PFC section

2.3.1 Crirical conduction mode PFC operation

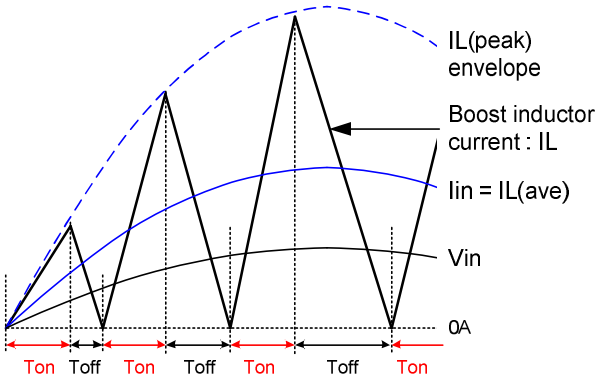


Fig.4 .Critical conduction mode operation

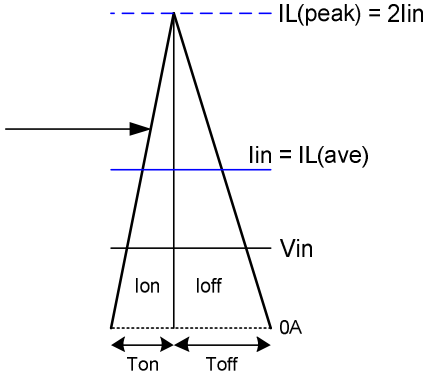


Fig. 5 . Switching one cycle

Boost inductor current is principally repetitive triangle waveform as shown in Fig.4.
Although Ton is constant in static condition (input AC voltage and output power) , Toff is varied according to sinusoidal input voltage. That results in large switching frequency variation.

Operaing current is calculated from formulas below.
Ton and L is constant , so peak value of IL : IL(peak) is proportional to input sinusoidal voltage Vin.
Vin is sinusoidal, so IL(peak) is also sinusoidal.（formula 1）

$$IL(peak) = \frac{V_{in} \times T_{on}}{L} \quad [A] \text{ - - - (1)}$$

Where switching frequency is much higher than input AC frequency (50 – 60Hz),so Vin can be estimated as constant dc voltage in one switching period. (Fig. 5)

Input current Iin is equal to avaraged PFC input current IL(ave).
また,IL is repetetive triangle , so IL(ave) equals to half value of IL(peak).（Formula 2）

$$I_{in} = IL(ave) = \frac{IL(peak)}{2} \quad [A] \text{ - - - (2)}$$

Substituting (1) to formula (2),

$$I_{in} = IL(ave) = \frac{IL(peak)}{2} = \frac{V_{in} \times T_{on}}{2L} \quad [A] \text{ - - - (3)}$$

Formula (3) shows Ton control can shape input current proportional to Vin, and resultly power factor can be simlpy corrected.
Basic waveform of PFC operation is shown in Fig. 6.

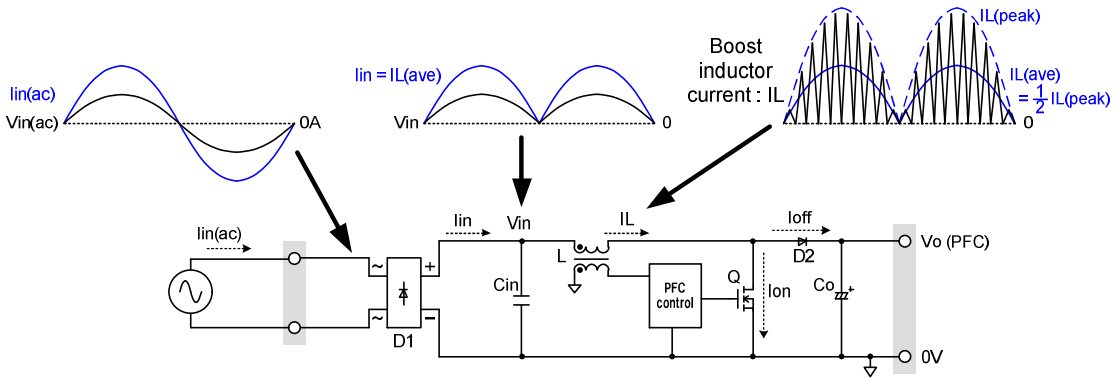


Fig.6 . PFC operation waveform

2.3.2 Zero Current sensing : ZC (pin 3)

MCZ5209SN VGP turn on timing is determined by boost inductor winding sensed pulse voltage applied to ZC terminal.
VGP turns on when ZC terminal voltage decreases below Vzc(L) of 0.5V as shown in Fig.7
As a result, demagnetization of boost inductor is completed at each switching period and PFC works in critical conduction mode.
Turn on threshold of 0.5V has 1V hysterisis to avoid undesired turn on cause by voltage ringing.
When there is no ZC pulse input as a initial state like startup transition, IC generates VGP output at every restart timing interval of Trestart 210us.
General CRM PFC has a disadvantage of too high switching frequency operation in light load condition. This causes turn on loss increase.
MCZ5209 limits too high frequency operation with bottom skipping function.
VGP output is disabled within 3.7usec after last cycle turn-off. If ZC turn on trigger appears in this period, IC skips gate output and waits for next trigger. As a result PFC works in bottom skip mode and turn on loss increase can be avoided.
Refer to section 3.1.5 also.

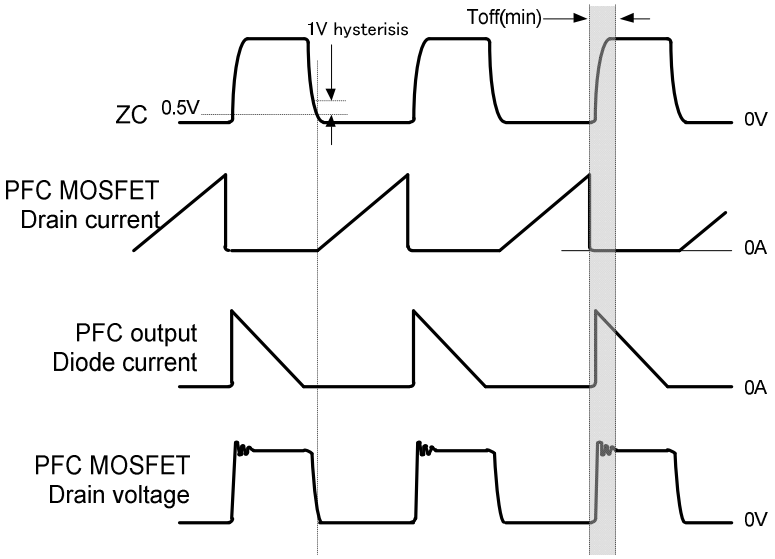


Fig.7 . PFC MOSFET ON tiniming (Z/C)

Table .4 ZC terminal **threshold** voltage and characteristics

description	symbol	condition	Typ. Spec.
ZC sensing threshold (H)	Vzc(H)		1.5 V
ZC sensing threshold (L)	Vzc(L)		0.5 V
Minimum OFF time	Toff(min)		3.7 us
Restarting interval	Trestart	ZC=0V	210 us

2.3.3 PFC output voltage sensing : FBP (pin 5)

MCZ5209SN stablizes PFC output by varing on period of PFC MOSFET sensing output DC voltage.
PFC output dc voltage is applied to FBP terminal using deviding resistor (R111-R114, R115), and stabilized when FBP terminal voltage reaches to Vo(ref) of 3.0V. (Fig.8)
Error amp output (COMP terminal voltage) and VGP ON period is proportional as shown in Fig.9.
Connect filter capacitor between FBP and GND, 1000pF – 2200pF is recommended.

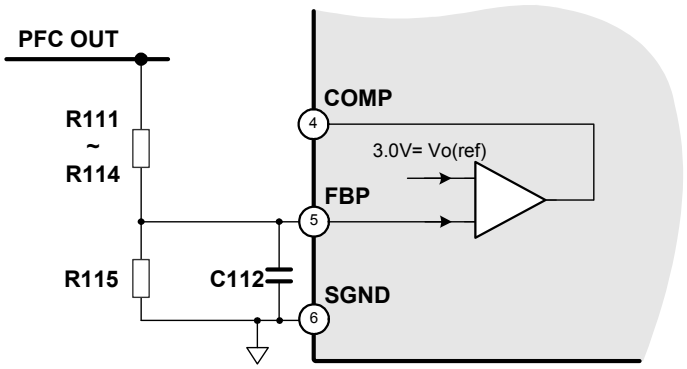


Fig.8. FBP connection and internal block

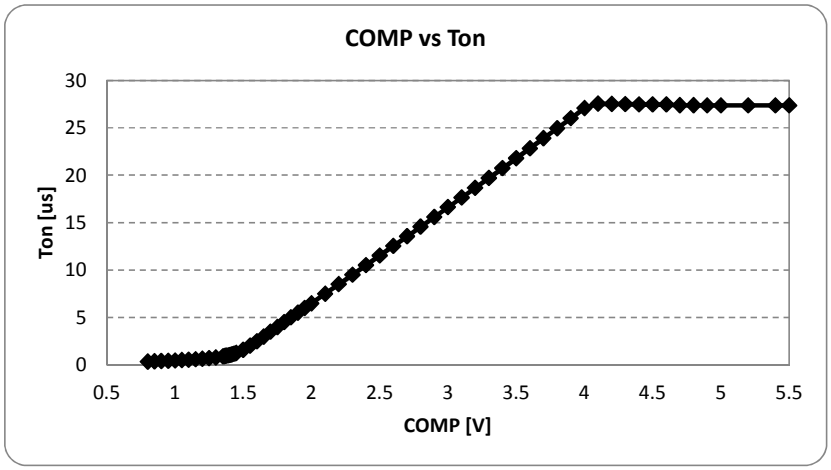


Fig.9 . COMP terminal voltage vs On time characteristics

Table .5 FBP ellectrical characteristics

parameter	symbol	condition	Typ. Spec.
Error amp input threshold	Vo(ref)		3.0 V
Minimum ON time	Ton(min)	COMP=Vth(bst)	300 ns
Maximum ON time	Ton(max)	COMP=open or 5V	27.5 us

2.3.4 PFC control phase compensation : COMP (pin 4)

PFC control characteristics should be adjusted not to response input AC frequency.
C / CR filter is used for phase compensation and gain adjustment.
Typical connection is shown in Fig.10. 1u – 2.2uF for C133 / 0.22u-0.47uF for C132
And 1k – 10k ohm dor R132 is recommended as the initial value.

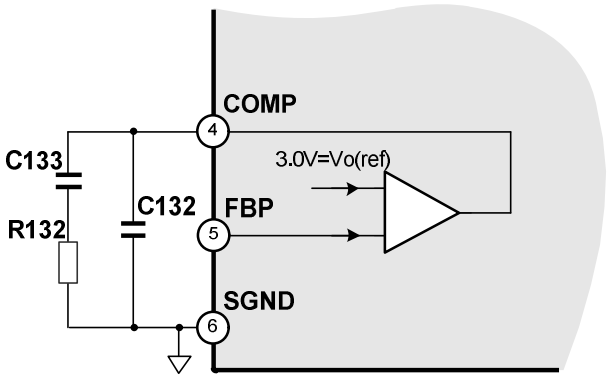


Fig.10 . COMP terminal connection

Table .6 COMP ellectrical characteristics

parameter	symbol	condition	typ.spec.
Error amp source current 1	Ieaso1	SST=0V,FBP=0.6V,COMP=3.0V	-100 uA
Error amp source current 2	Ieaso2	SST=2.4V,FBP=0.6V,COMP=3.0V	-50 uA
Error amp sink current	Ieasi	FBP=5.0V,COMP=3.0V	100 uA
Burst mode entering threshold	Vth(bst)		0.8 V

2.3.5 PFC gate driver : VGP (pin 1)

Voltage source of gate driver is internally stabilized (Vc2) and drive capability of 0.58A(Source)/0.6A(Sink) enoughly suppresses undesired drive or control malfunctions caused by sharp gate driving current.

General gate drive connection is shown in Fig.11.
R1 and R2 according to desired MOSFET gate drive condition.

Sourcing resistor (Rsrc) = R1 (A) / R1+R2 (B) (C)
Sinking resiatance (Rsink) = R2 (A) (C) / R1 (B)

Snappy (hard recovery) diode is not recommended for gate sinking use as shown in Fig.11 A),B).
Soft recovery type or low voltage SBD is recommended like :
D1NS4 (axial) , M1FM3 (SMD) --- Shindengen

PNP BJT sinking is effective when using large Qg MOSFET as shown in Fig. 11 (C).

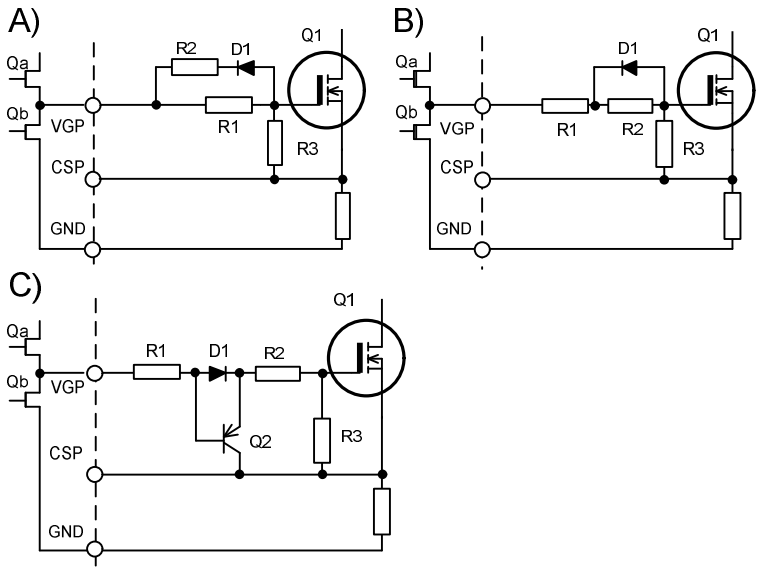


Fig.11. PFC gate drive connection

Table .7 PFC gate drive capability

parameter	symbol	condition	Typ. Spec.
Sourcing current	Iout(so)P	Vc2=VB=13V , VGP=0V	-580 mA
Sinking current	Iout(si)P	Vc2=VB=13V , VGP=13V	600 mA

2.3.6 PFC protection

2.3.6.1 PFC Over current limiter : CSP (pin 2)

PFC MOSFET source current is sensed by current sensing resistor connected between MOSFET Source terminal and primary ground. Sensed voltage is applied to CS terminal as shown in Fig.12.

VGP output is disabled instantaneously when CSP terminal voltage exceeds Vcsp 0.5V. Operating point should be designed considering minimum input AC and maimum output powercondition.
OCP does not work during Leading Edge Blanking time (TLEB) to avoid undesirable OCP operation caused by turn surge current. (Fig.13)
Insert R/C filter to avoid malfunction between CSP and GND. (Fig.12)
1000p-10000pF for C121 and 47ohm – 1k ohm for R126 is recommended.

See also section 3.1.8.

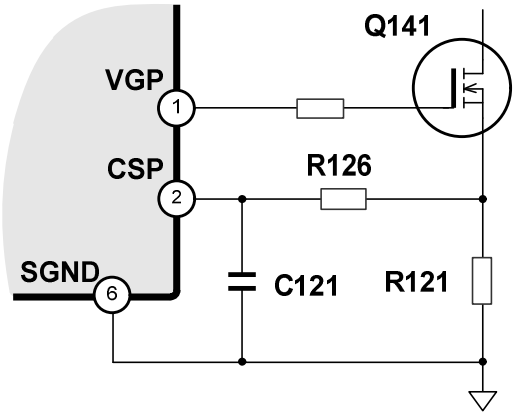


Fig.12 . CSP connection

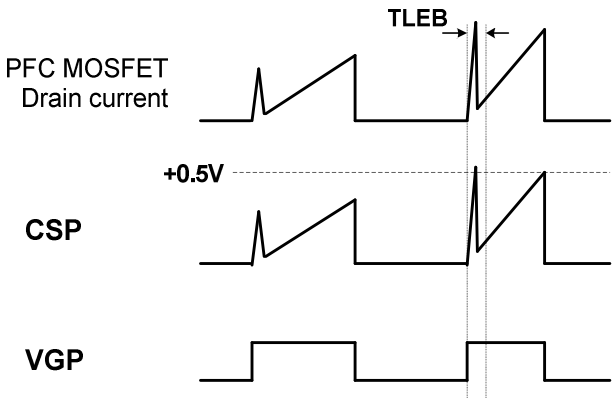


Fig.13 . OCP operation timing

Table .8 CSP ellectrical characteristics

parameter	symbol	condition	Typ. Spec.
Input threshold	Vcsp	FBP=1.0V	0.5 V
Leading edge blanking time	Tleb	CSP=1.0V	400 ns

2.3.6.2 output voltage protection
(dynamic OVP / input UVLO / PFC loop open protection)

[Dynamic OVP]
VGP output is disabled when FBP terminal voltage exceeds Vo(ref)×1.08 and avoid output voltage excess overshoot to protect output capacitor.

[Input UVLO]
VGP output is disabled when FBP terminal voltage decreases to Vfbp(off) 0.35V and is enabled when voltage exceeds Vfbp(on) 0.45V again.

[Loop open protection]
Input UVLP also works as loop open protection.
When FBP sensing loop is opened or FBP – GND shorted, VGP output is disabled instantaneously.

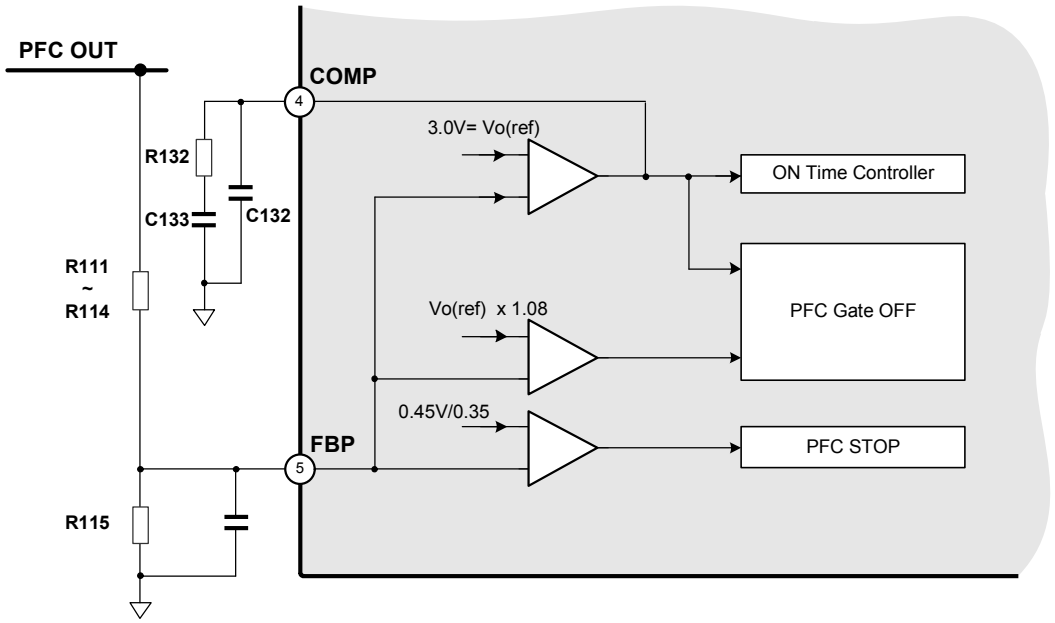


Fig.14 . FBP connection and internal block

Table .9 PFC protection ellectrical characteristics

parameter	symbol	condition	Typ. Spec.
FBP ovp threshold	Vfbp(H)		Vo(ref)*1.08 V
FBP loop open /UVLO threshold 1	Vfbp(on)		0.45 V
FBP loop open /UVLO threshold 2	Vfbp(off)		0.35 V

2.4 LLC section

2.4.1 Oscillator and Feed Back : FBL (pin 12)

MCZ5209SN operating frequency is determined by charging and discharging time of timing capacitor Ct connected FBL terminal.
Ct discharging period is the ON period of VGH / VGL, and Ct charging time is the OFF period of VGH / VGL (= Dead Time).
FBL triangle waveform works in double frequency of LLC converter operating frequency and VGH and VGL output is enabled alternately between dead time.
Operation timing is shown in Fig.15.
Ct charging start threshold is changed according to LLC operation mode of symmetric mode and asymmetric mode as shown in Fig.16.

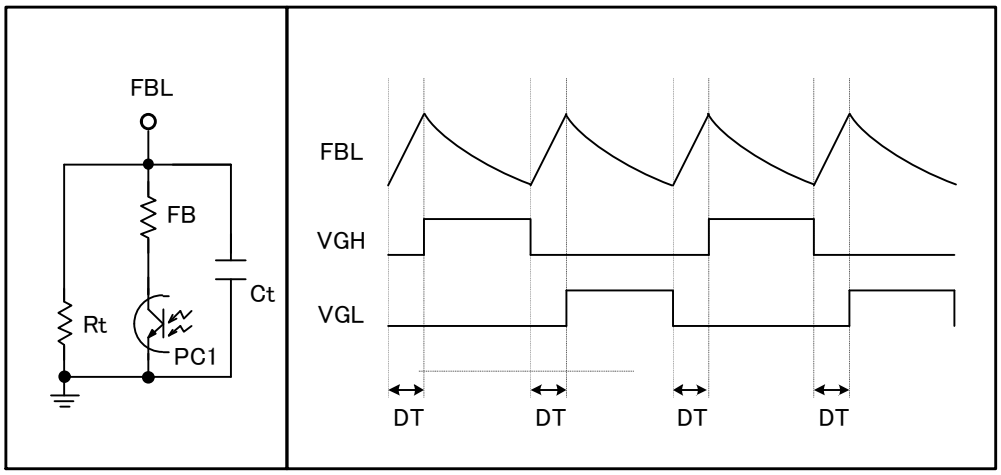
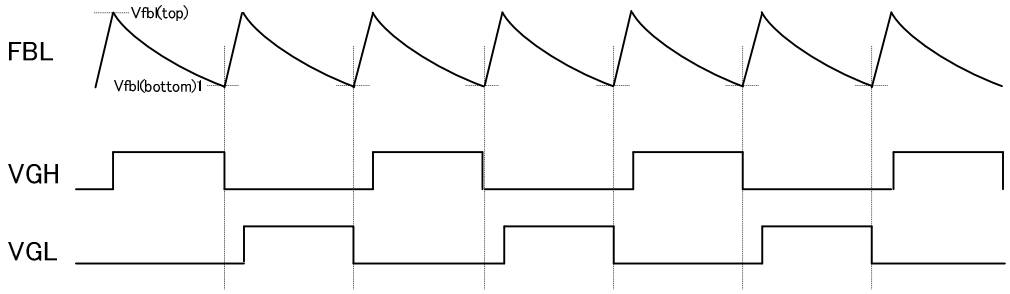
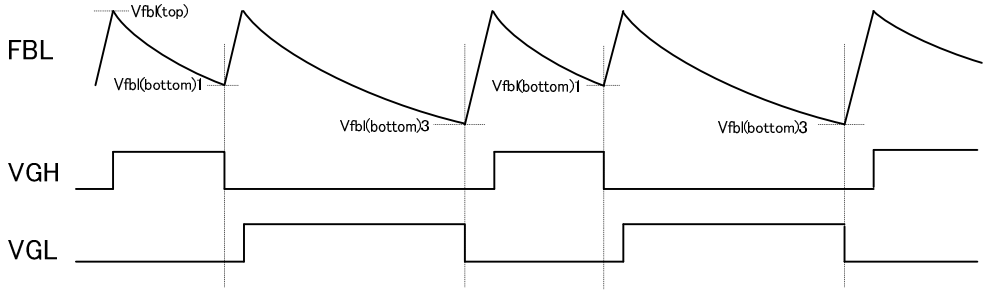


Fig.15. FBL connection(a) Operating timing (b)



(A) Normal mode (symmetrical LLC)



(B) Active stdby mode / Burst mode (asymmetrical LLC)

Fig.16. Gate drive timing of symmetric/asymmetric operation

Control optocoupler PC1 is connected to FBL terminal through FB resistor.
When PC1 current increases, operating frequency increases due to decrease of Ct discharging period and vice versa.
Component value and frequency / dead time characterics are shown in Fig.17.

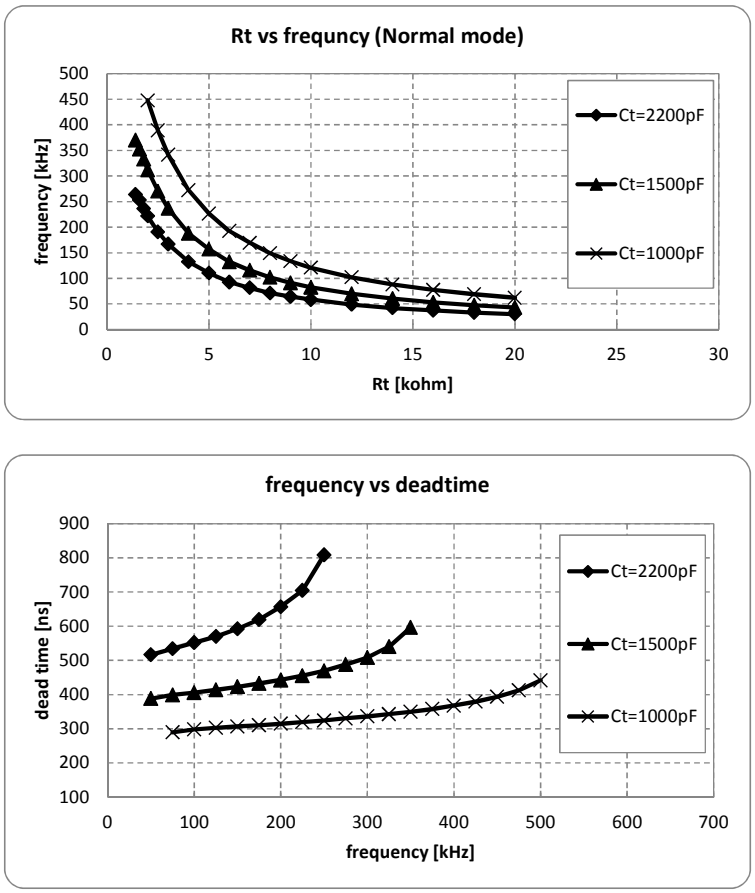


Fig.17. Rt vs frequency (upper) frequency vs dead time (lower) characteristics

Table .10 FBL ellectrical characteristics

parameter	symbol	condition	Typ.spec.
FBL sourcing current	Ifbl(charge)	FBL=4.0V	-9.0 mA
FBLsourcing stop threshold	Vfbl(top)		4.75 V
FBL charing start threshold 1	Vfbl(bottom)1		3.4 V
FBL charing start threshold 2	Vfbl(bottom)2	Tss(3)	2.4 V
FBL charing start threshold 3	Vfbl(bottom)3	ASTBY=open	2.3 V

2.4.2 LLC Gate driver VGH,VGL (pin 22,16)

VGL drives low side MOSFET gate and VGH drives high side.
0.23A sourcing and 0.38A sinking capability is enough for middle power application avoiding undesirable operation caused by surge current of gate driving.

Gereral gate drive connection is shown in Fig.18(A).
Single resistor drive is enough in 100-200kHz operation with Qg 20-30nC MOSFET.
When using large Qg MOSFET,Sinking diode is effective to speed up turn off as shown in Fig.18 (B),(C).
Snappy (hard recovery) diode is not recommended for sinking diode use,
Soft recovery or small SBD is recommended like :
D1NS4 (axial) , M1FM4 (SMD) – Shindengen

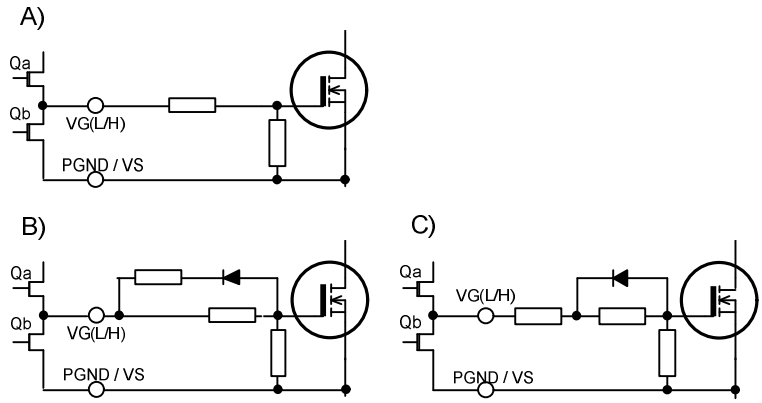


Fig.18. LLC gate drive connection

High side floating voltage for high side drive (VB) is gererated by boot strapping circuit from Vc2 shown in Fig.19.

External bootstrap diode D233 connection achieves small difference between Vc2(low side gate drive voltage) and VB(high side gate drive voltage) and stable converter operation is assured by internally stabilized Vc2 voltage even in input/output transient condition or abnormal condition.

0.1u – 1uF MLCC is recommended for C239,and 600V soft recovery type FRD is recommended
For bootstrap diode D233 like D1NK60(axial) or D1NF60(SMD) – Shindengen.
Please take care of D233 creepage distance.

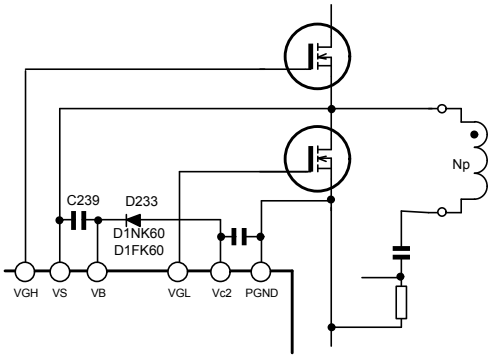


Fig.19. Boot strap for high side floating drive

Table .11 LLC gate driver capability

parameter	symbol	condition	Typ. Spec.
Sourcing current	Iout(so)L	Vc2=VB=13V , VGL=VGH=0V	-230 mA
Sinking current	Iout(si)L	Vc2=VB=13V , VGL=VGH=13V	380 mA

2.4.3 LLC protections

2.4.3.1 LLC OCP/OLP/Capacitive mode protection CSL,CSO (pin 11,10)

Primary resonant current is sennsed by sensing resistor or sensing capacitor.Sensed voltage is applied to CSL terminal for current and capacitive mode protection use of MCZ5209SN
Fig.20 shows an example connection of resistor sensing case.

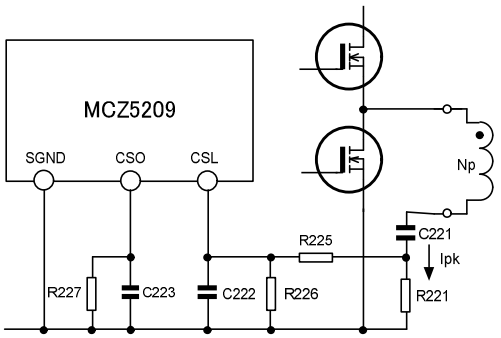


Fig.20. CSL and CSO connection

R221 is the main sensing resistor, and sensed voltage is applied to CSL terminal through R/C filter.
R226 is a voltage divider to adjust OCP operating point.
Component value setting is described in section 3.2.5.

CSL terminal has three threshold voltages for independent protections as shown in Table 12.

Table .12 Tree functions of CSL terminal

	symbol	function	CSL threshold voltage
1	OCP1	Cycle by cycle OCP	CSL >+0.525V or < -0.525V
2	OCP2	Frequency limit OLP	CSL >+0.35V or < -0.35V
3	di/dt	Capacitive mode protection	CSL <+0.07V or > -0.07V

*OCP : Over current protection , OLP : Over load protection

[OCP1]

OCP1 cycle by cycle current protection operates when CSLvoltage terminal exceeds +/-0.525V.
Specifically, +0.525V in high side MOSFET ON period and -0.525V in low side MOSFET ON period.
Fig.21 shows operation timing example of OCP1 operation during high side MOSFET ON period.

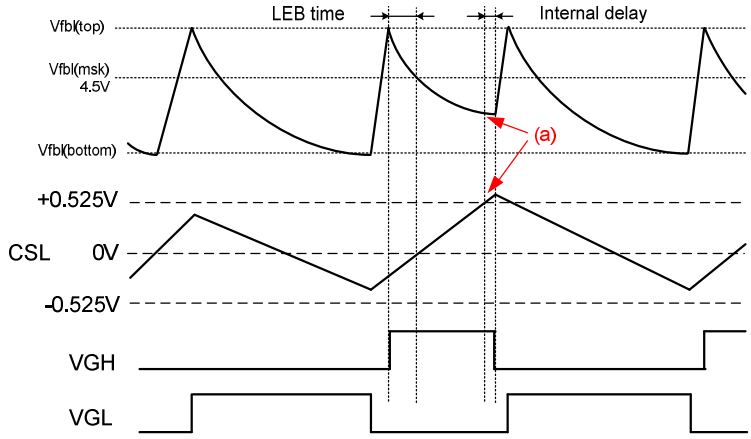


Fig. 21. OCP1 operation timing

When OCP1 operates, MCZ5209SN behavior is as follows :

(a) FBL starts Ct charging and diables VGH/VGL output instantenuously.

(b) SST capacitor starts to be charged by 40uA for eight cycle of FBL triangle.

(c) CSO capacitor starts to be charged by 750uA for eight cycle of FBL triangle.

Cycle by cycle fast protection prevents excess current flow of MOSFET or inductor saturation under abnormal condition like load short, winding short or output diode short. And timer delayed lathing protection prevents overheat of winding or output diode in load short condition.

If OCP1 is not triggered within 8 cycle of FBL triangle, SST capacitor is discharge by Itimer(refresh) of 650uA until SST terminal voltage decreases to 2.1V.

[LEB]

LEB (Leading Edge Blanking) time is inserted to avoid undesirable OCP1 operation caused by hard switching turn on surge current or surge voltage due to parasitic inductances. OCP1 never operates even if CSL terminal voltage exceeds +/-0.525V during LEB period.

[internal filter]

200nsec filter is inserted in FBL voltage sensing loop to prevent oscillator malfunction , so OCP1 operation has a few hundred nsec delay including OCP comparator response.

[OCP2]

OCP2 operates when CSL terminal voltage exceeds +/-0.350V.

When OCP2 operates,MCZ5209SN behavior is as follows :

(a) SST capacitor is charged during 8 cycle of FBL triangle. Charging current is varied accordingto CSO terminal voltage.

- 0.9V ≤ CSO < 1.0V : SST charging desabled
- 1.0V ≤ CSO < 1.5V : SST charging current is set to 1.7uA
- 1.5V ≤ CSO ≤ 2.5V : SST charging current is set to 40uA

(b) CSO capacitor is charged by 750uA

LEB is also effective for OCP2.

If OCP2 is not triggered within 8 cycle of FBL triangle after last OCP2 detection, SST capacitor is discharge by Itimer(refresh) of 650uA until SST terminal voltage decreases to 2.1V.

[CSO]

In OCP2 operation, LLC operating frequency is varied according to CSO terminal voltage.
Voltage and frequency characteristics are shown in Fig.22.
CSO capacitor is pre-charged to 0.9V initially, Frequency shift begins when CSO terminal voltage exceeds 1.0V and operating frequency increases according to terminal voltage increase.
As a result, output power is limitted.
Please notice power limitting point and frequency relationship closely depends on resonant condition (inductance ratio and operation mode of CRM / CCM / DCM).

Charging maximum voltage of CSO is 2.5V.

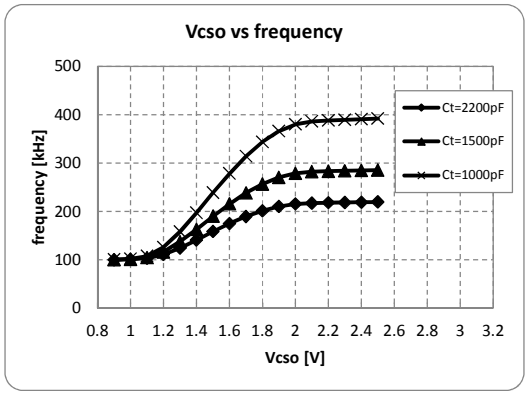


Fig.22 CSO voltage vs frequency

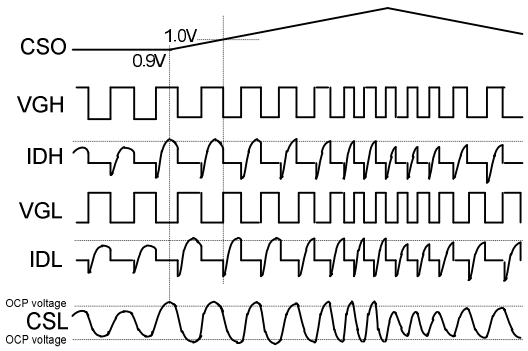


Fig.23 OCP2 timing

[Capacitive mode protection (di/dt protection)]

di/dt protection operates when CSL terminal voltage decreases to +/-0.070V.
Specifically, +0.07V in high side MOSFET ON period and -0.07V in low side MOSFET ON period.

When di/dt protection operates,MCZ5209SN behavior is as follows :

(a) FBL starts Ct charging and diables VGH/VGL output instantenuously.

(b) SST capacitor is charged according to IC opetaing mode
- Normal mode : SST charging is disabled
- Active stdby mode : charging current is set to 40uA during 8 cycles
- Burst mode : charging current is set to 40uA during 8 cycles

Fast cycle by cycle operation prevents most dangerous capacitive mode stress of MOSFETs.
Please notice generic switching loss calculation and transient Tj estimation have no meaning for MOSFET capacitive mode stress.

LEB is also effective for di/dt protection.

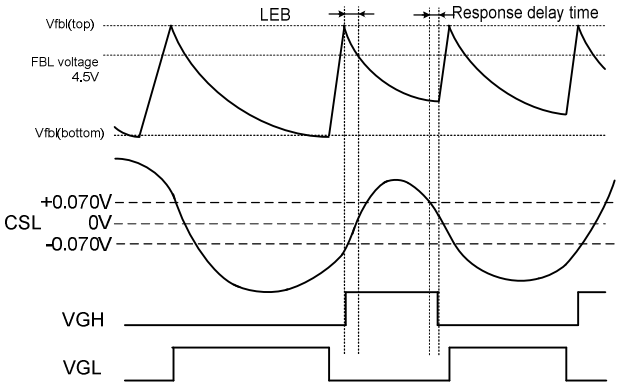


Fig.24. Capacitive mode protection timing

Table 13 shows the SST and CSO charging status according to each protection and LLC operating mode.

Table .13 SST and CSO charging status

Detection mode	Operation mode	SST charging	CSO charging
OCP1	Normal mode	(A)	(B)
	Active stdby mode		
	Burst mode		
OCP2	Normal mode	(C)	(D)
	Active stdby mode		
	Burst mode		
Capacitive mode (di/dt)	Normal mode	N.A.	N.A.
	Active stdby mode	(A)	
	Burst mode	(A)	

(A) SST capacitor is charged by 40uA during 8 cycle of FBL triangle
(B) CSO capacitor is charged by 750uA during 8 cycle of FBL triangle
(C) SST capacitor is charged by 1.7uA(1V ≤ Vcso < 1.5V),40uA(1.5V ≤ Vcso)
(D) CSO capacitor is continuously charged by 750uA if CLS terminal voltage exceeds OCP2 threshold

Table .14 CSL / CSO terminal thresholds

parameter	symbol	condition	typ.spec.
CSL voltage of OCP1(+/-)	Vocp1(+/-)		+/- 0.525 V
CSL voltage of OCP2(+/-)	Vocp2(+/-)		+/- 0.350 V
CSL voltage of di/dt(+/-)	Vdidt(+/-)		+/- 0.070 V
CSO terminal pre-charging	Vcso(pre)	CSL=0V	0.90 V
CSO voltage (freq shift start)	Vcso(ocp2)	lVocp2(+/-) l< CSL < lVocp1(+/-)l	1.0 V
CSO voltage for SST charging current switch	Vcso(tmr)		1.5 V
CSO charging current	Icso(ocp2)		-750 uA

2.4.3.2 Brown out protection : FBP (pin 5)

Input brown out protection for LLC converter is performed by using FBP terminal voltage.
SST capacitor is charged or discharge according to FBP terminal voltage level.

Operating threshold is switched according to IC operating mode as shown in Table 15.

Table .15 FBP terminal threshold by exach operating mode

Operation mode	SST charging	SST discharging
Normal mode	2.2V	2.0V
Active stdby mode	0.65V	0.55V
Burst mode	0.65V	0.55V

Table .16 Brown out threshold

parameter	symbol	condition	typ.spec.
Brow out threshold 1(on)	Vsen1(ss-reset)	Normal mode	2.2 V
Brow out threshold 2(off)	Vsen2(ss-reset)	Normal mode	2.0 V
Brow out threshold 3(on)	Vsen3(ss-reset)	AS mode/Burst mode	0.65 V
Brow out threshold 4(off)	Vsen4(ss-reset)	AS mode/Burst mode	0.55 V

2.4.3.3 SST terminal (pin 13)
(Soft start timing / Safe startup / Timer delay protection timing)

SST terminal is assigned to four functions as follows :

(1) Soft starting
(2) Safe startup (startup di/dt protection : Tss(3))
(3) protection Delayed timer
(4) Timer delayed latching

(1) Soft start

MCZ5209 adopts generic LLC soft start function of Frequency shift from high frequency decreasing to stabilized frequency as shown in Fig.25.

SST charging starts when three conditions are satisfied as followings :
(a) Vc2 terminal voltage ≥ 10.0V AND
(b) LS terminal voltage ≥ 2.0V AND
(c) FBP terminal voltage ≥ specified threshold (described in Table 15)

SSTоperation timing is shown in Fig.26.
FBL osillator starts generating refernce triangle when SST terminal voltage exceeds 0.6V.
Initial Startup frequency fss is determined by Ct value. This frequency can be independent from LLC maximum frequency fmax.
SST terminal is clamped to 2.1V after startup period ended unless protection operation starts.

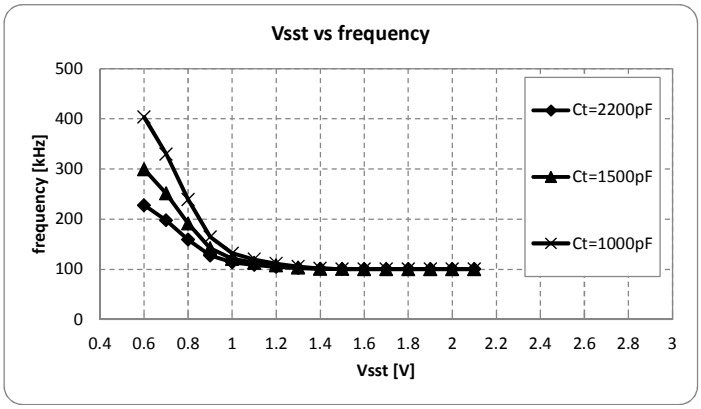


Fig.25 SST voltage and operation frequency

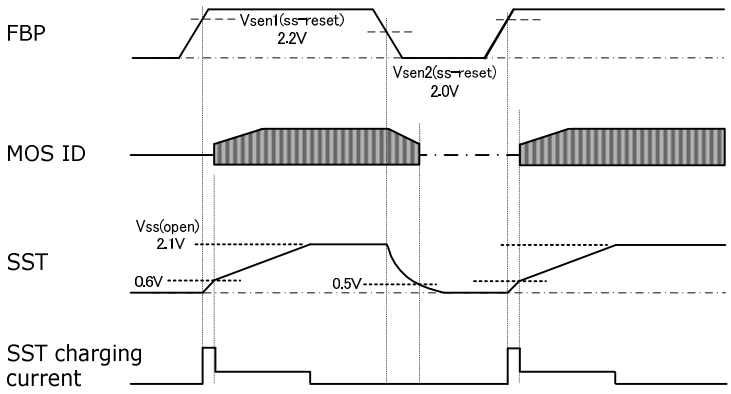


Fig.26 SST operation timing

(2) Safe startup Tss(3)

MCZ5209SN has safe startup function to suppress body diode didt mode in beginning of startup period.

Resonant capacitor applied voltage is unstable in the beginning period just after LLC startup.
In this period conventional gate driving has possibility of MOSFET body diode didt stress.
MCZ5209SN starts with slightly unbalanced non symmetrical drive to quicken convergence of resonant capacitor voltage and unbalanced resonant current enters stable operation as shown in Fig.27.

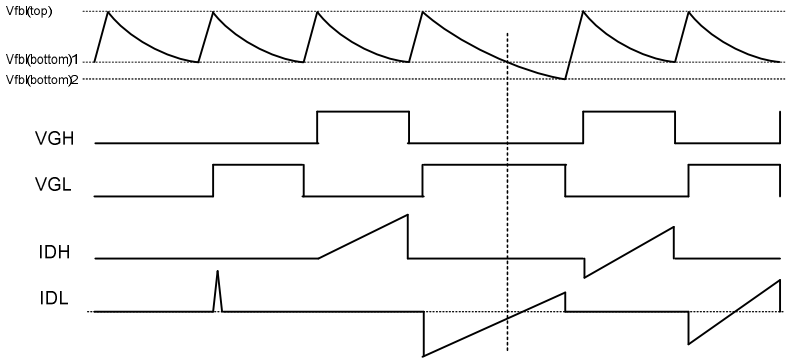


Fig.27 Safe startup : Tss(3) timing

(3) Timer delayed latching protection

MCZ5209SN has timer delayed latched protection mode.
Refer to Table 13 and Fig.28 to confirm Timer charging condition and timing.
SST capacitor charging start when abnormal condition is detected like OCPs.
Charging curent is switched acdcording to LLC operating mode as shown in Table 13.

OCPs triggers SST capacitor charging. IC output is disabled when SST terminal voltage reaches to 3.5V and SST capacitor starts to be discharge by 6.7uA, and IC restarts operation automatically when SST terminal voltage decreases to 0.3V.

Latch counter is built in to prevent undesirable latching. Even if timer delayed off protection worked with one protection cycle,IC resumes normal operation once abnormal condition is removed. Continuous latching works only after twice couning of continuous abnormal condition.
Continuous latched status is released when Vc2 voltage decreases to 7.5V.

Detailed operation timing is shown in Fig.28

Condition (A) :
Abnormal condition (like over load) is removed before SST terminal voltage reached to 3.5V.
SST capacitor starts to be discharged by 650uA just after abnormal condition is removed,
VGH/VGL is not disabled and Latching status is not counted.

Condition (B) :
IC output is disabled when SST terminal voltage reaches to 3.5V and latching mode is counted,SST capacitor starts to be discharged by 6.7uA until SST terminal voltage decreases to 0.3V.
SST terminal voltage increases again and VGH/VGL is enabled when voltage exceeds 0.6V.
When abnormal condition is not detected at the instant of SST = 1.5V , latching counter is initialized and operation restarts .

Condition (C) :

When abnormal condition is not removed continuously, IC enters into latching stop mode and PFC output is also disabled.

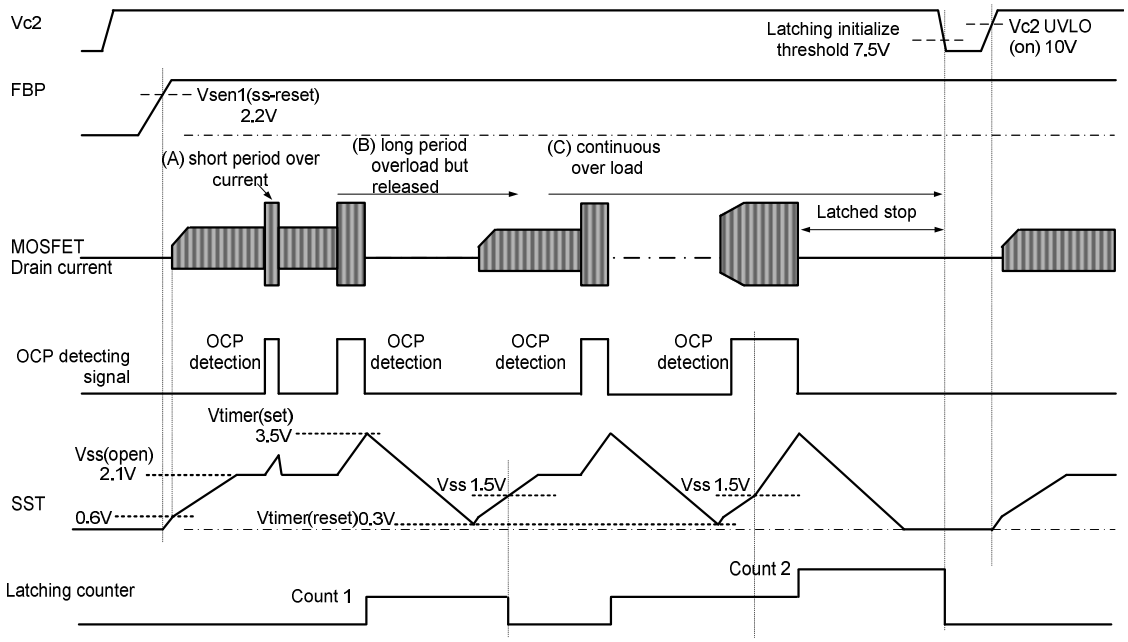


Fig.28 SST timer delayed latching timing

Table .17 SST terminal threshold

parameter	symbol	condition	typ.spec.
LLC enable threshold	Vss		1.5 V
SS charging current1	Iss(charge)1	SST=0V	-90 uA
SS charging current 2	Iss(charge)2	SST=1.0V	-30 uA
SS discharging current	Iss(discharge)	SST=1.0V FBP=0V	180 uA
SST open voltage	Vss(open)		2.1 V
LLC starting SST voltage	Vss(st)		0.6 V
LLC stop SST voltage	Vss(sp)		0.5 V
Timer **threshold** 1(off)	Vtimer(set)		3.5 V
Timer **threshold** 2(reset)	Vtimer(reset)		0.3 V
Timer charging current 1	Itimer(charge)1	CSL > IVocp1(+/-)I	-40 uA
Timer charging current 2	Itimer(charge)2	Table 13	-1.7 uA
Timer charging current 3	Itimer(charge)3	Table 13	-40 uA
Timer discharging current (Refresh)	Itimer(refresh)		650 uA
Timer discharging current (interval)	Itimer(discharge)		6.7 uA

2.5 Common section

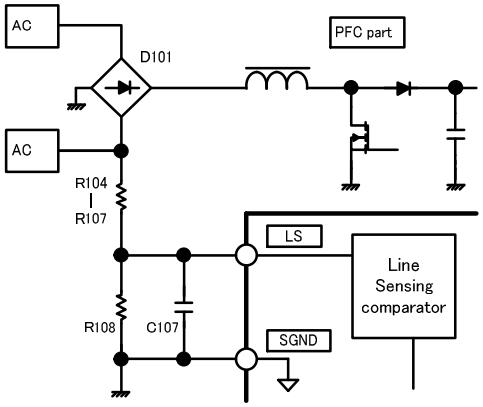
2.5.1 AC Line Sensing : LS (pin 7)

LS terminal is a line sensing input to control PFC and LLC operation status according to line input voltage.

PFC and LLC operation is enabled when LS terminal voltage exceeds 2.0V as shown in Fig.30.

When LS terminal voltage is less than 2.0V or decreases to 1.5V after exceeding 2.0V, COMP capacitor,SST capacitor,Vc1 capacitor and BURST capacitors are discharged.

LS function can be used as input low voltage protection or another protection wit external signal.



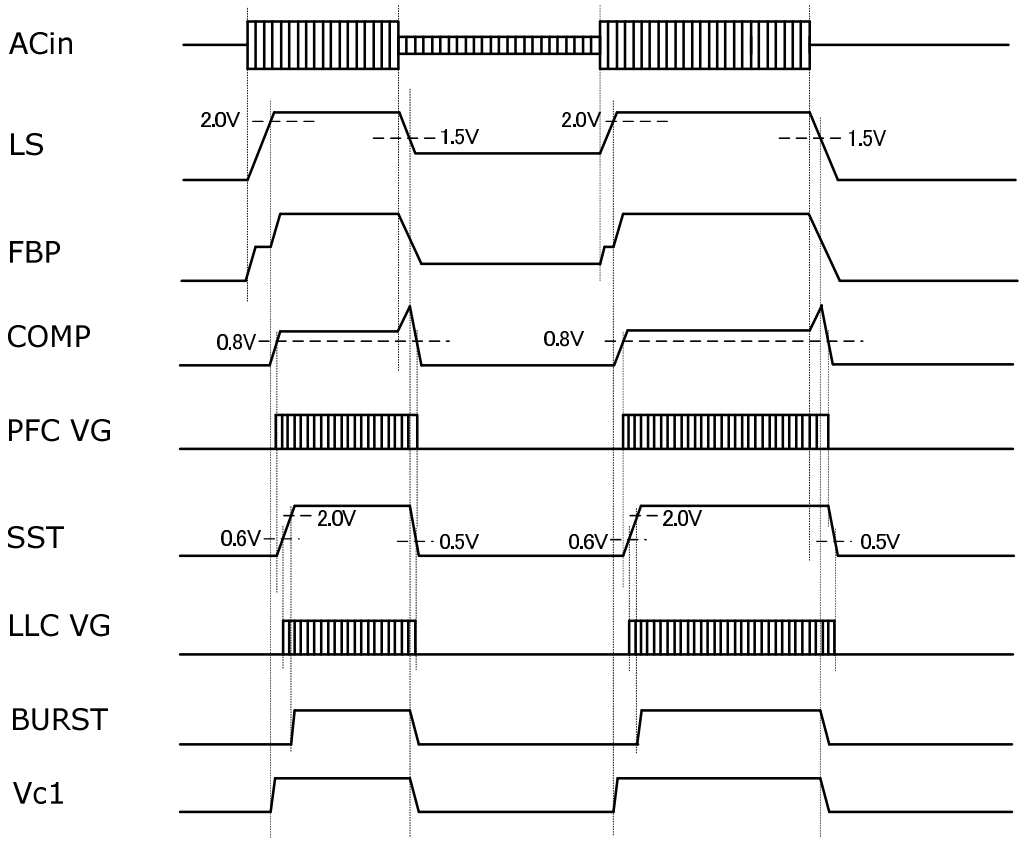


Fig.30 Line sensing timing

Table .18 LS terminal ellectrical characteristics

parameter	symbol	condition	typ.spec.
LS shreshold (VGP/VGH/VGH enable)	Vls(st)	Vin=Vc1=24V	2.0 V
LS shreshold (VGP/VGH/VGH disable)	Vls(sp)	Vin=Vc1=24V	1.5 V
BURST terminal dischargig current (LS off)	Ibst(lsdis)	Vin=Vc1=24V , LS=0V	4.5 mA
Vc1 terminal discharging current (LS off)	Ivc1(lsdis)	Vin=Vc1=24V , LS=0V	1.8 mA

2.5.2 Active stdby and burst mode

IC operating mode is determined by ASTBY terminal voltage
Operation status and operatin mode according to ASTBY voltage is shown in Table 19.

Table .19 ASTBY terminal voltage vs operation mode

ASTBY terminal voltage	Operating mode	PFC	LLC
0V ≤ ASTBY < 1.0V	Normal mode	enabled	Symmetric
1.0V ≤ ASTBY < 3.2/3.0V	Asymmetric step mode	enabled	Asymmetric
3.2/3.0V ≤ ASTBY < 4.0/3.9V	Active stdby mode	disabled	Asymmetric
4.0/3.9V ≤ ASTBY ≤ 4.5V	Burst mode	disabled	Asymmetric

2.5.2.1 Active stdby ASTBY (pin 8)

Active stdby mode is asymmetric LLC operation mode to improve light load efficieny reducing magnetizing current.In this operating mode VGL on period is expanded to duty ratio of VGH and VGL reaches to 1 : 2. Detail timing is shown in Fig.31.

IC operates in normal mode when ASTBY terminal voltage is less than 1V as shown in table 19 and enters into LLC acymmetric step mode at ASTBY terminal voltage is from 1V to 3.2V.In this mode, asymmetry is varied according to ASTBY terminal voltage, from 1:1 to 1:2.PFC is not disabled during this mode.
PFC is disabled and LLC enters into fixed asymmetric operation mode when ASTBY terminal voltage exceeds 3.2V. To restart to asymmetric step mode, sink ASTBY terminal to less than 3.0V. When entering into active stdby mode, brown out protection threshold voltage is switched from 2.2V/2.0V to 0.65V/0.55V and Timer charging is enabled by didt protection.

In restart from active stdby mode to asymmetric step mode period, brownout threshold voltage is switched from 0.65V/0.55V to 2.2V/2.0V after FBP terminal voltage exceeds AS mode reset masking voltage of 2.4V.

2.5.2.2 Burst mode operation ASTBY,BURST,SSC (pin 8,9,14)

IC enters into Burst mode when ASTBY terminal voltage exceeds 4.0V. ASTBY terminal voltage should be 3.9V or less to reset burst mode to continuous mode.
SSC terminal is opened during burst mode to shorten startup period. In normal mode snd active stdby mode, SSC capacitor is sinked by 5mA.

BURST terminal is sinked internally by Ibst(dis)1 of 400uA in normal mode and active stdby mode, This internal current sinking is disabled when IC enters into burst mode.

Generally sensed dividing voltage from Vc1 or external signal is applied to BURST terminal, SST capacitor is discharged and LLC operation enters into halt mode when BURST terminal voltage exceeds 2.0V and SST capacitor charging starts and LLC operation restarts when BURST terminal voltage decreases to 1.8V .
Timing detail is shown in Fig.31.

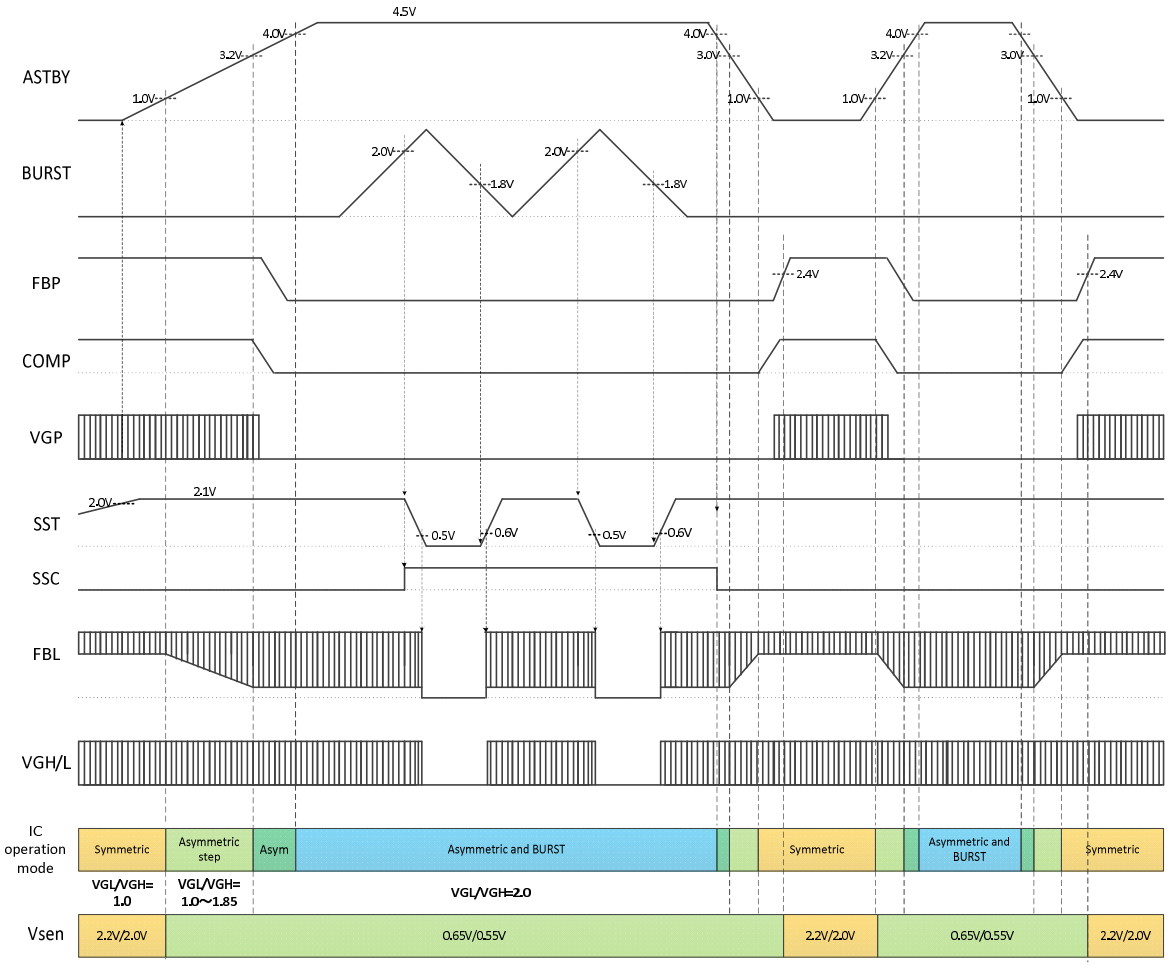


Fig.31 Active stdby mode and Burst mode timing .

Table . 20 ASTBY,BURST terminal threshold

項目	symbol	condition	typ.spec.
ASTBY open voltage	Vastby(open)	Vin=Vc1=24V,SST=2.5V	4.5 V
ASTBY threshold (Burst enable)	Vastby(bston)		4.0 V
ASTBY threshold (Burst disable)	Vastby(bstoff)		3.9 V
BURST threshold (LLC disable)	Vbst(H)		2.0 V
BURST threshold (LLC enable)	Vbst(L)		1.8 V
ASTBY threshold (step symmetry start)	Vas(stpon)		3.0 V
ASTBY threshold (step symmetry end)	Vas(stpoff)		1.0 V
ASTBY threshold (AS mode enable)	Vas(on)		3.2 V
ASTBY threshold (AS mode disable)	Vas(off)		3.0 V
BURST discharing current 1	Ibst(dis)1	ASTBY<Vastby(bston/off) BURST=1.5V	400 uA
BURST discharing current 2(burst mode)	Ibst(dis)2	ASTBY>Vastby(bston/off) BURST=1.5V	0 uA
SSC discharging current	Issc(dis)	ASTBY<Vastby(bston/off) SSC=0.5V	5 mA

[External burst / active stdby selecting circuit example]

Additional circuit example of primary sensing burst and active stdby selection by external signal case is shown in Fig.32. refer section 3.3.3 for component value selection.

Fig.32 circuit consists of two functional section.
(A) is for burst interval adjustment and output voltage bottom limitting.
(B) is for operating mode selection.

[Section (A)]
C233 and 232 determines burst off time interval. Larger capacitance increases off period during burst operation. BURST operation ON/OFF timing is adjusted by R231 and R232 value. BURST terminal is internally sinked by 400uA during normal mode and Active stdby mode, so too small R231 /232 value causes undesirable LLC gate disable during normal mode and Active stdby mode operation due to BURST terminal voltage exceeding 2.0V. larger than 5k ohm is recommended as R231.

Secondary circuit of Fig.32 (A) block is for output voltage bottom limitting. Desired bottom voltage is determined by R384 and R385. When bottom of output voltage reaches to setting voltage,IC302 cut offs and Q301 is biased to lead diode current of opto coupler PC203. Thus BURST terminal voltage is sunk to force LLC operation start.

[Section (B)]
IC operation mode selection by external signal example.

Table . 20 STBY,AS signal and operating mode

	STBYsignal	AS signal	Operating mode
2	Low	High	Normal mode
3	High	Low	Active stdby mode
4	High	High	Burst mode

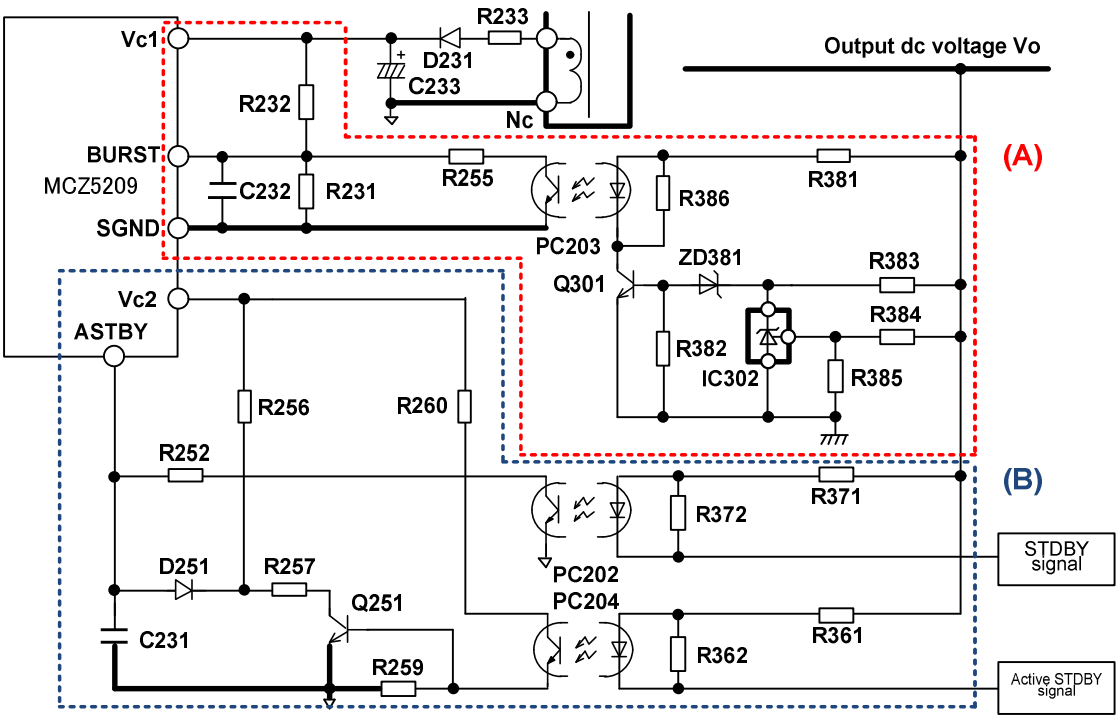


Fig.32. External AS / Burst selection circuit

2.5.3 Termal shutdown

MCZ5209SN has TSD (thernal shutdown) protection internally. Operating temperature is 140°C with 40 °C hysterisis. VGP/VGH/VGL output is disabled when TSD worked to prevent overheating.

3 Selection of component value

Component selection process is described hereafter. Fig.33 shows an example of self-biased single output LLC with active stdby and burst mode by external signal. Refer to Fig.45 also that shows self-biased LLC without active stdby and burst mode.

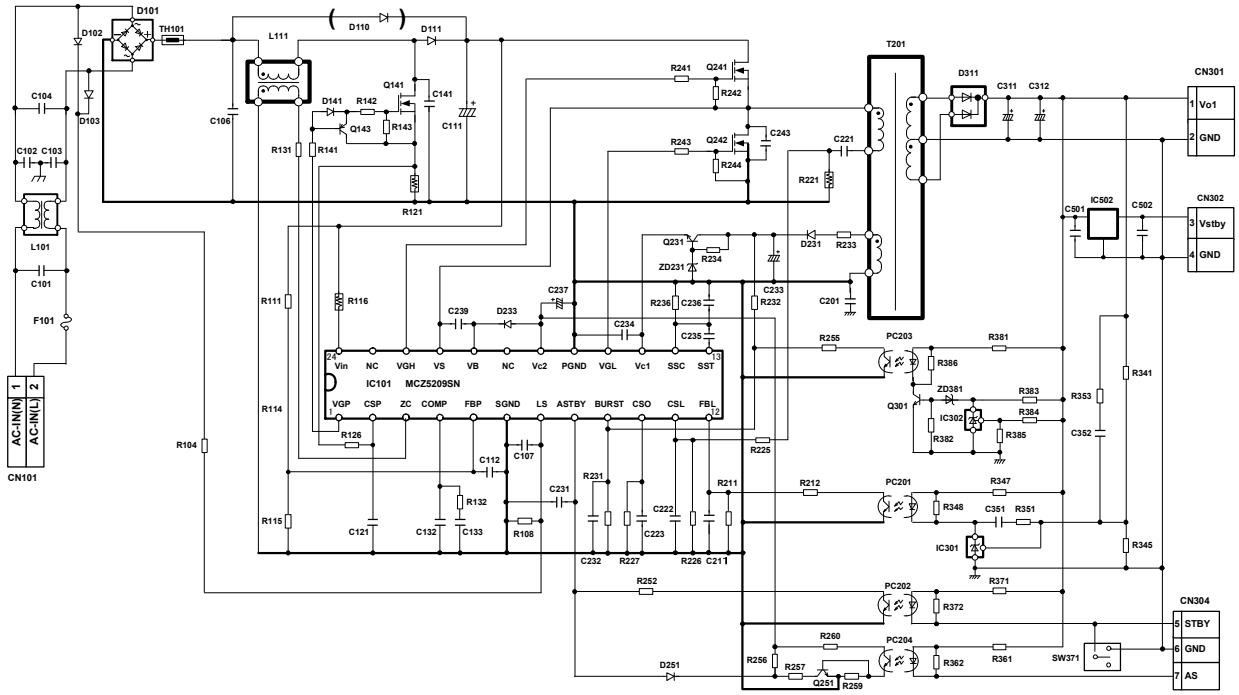


Fig.33. MCZ5209SN with active stdby and burst mode example

3.1 PFC section

3.1.1 PFC boost inductor

Following is general method of PFC boost inductor design.
Po : PFC nominal output power
Po(max) : PFC maximum output power
Ps : PFC output power at OCP operating point
generally 1.2 – 1.5 x Po(max)

< selection of core >
Core gap is generally less than 2mm considering winding loss caused by leakage flux.

$$lg = 4\pi \times \frac{Ae \times Np^2}{Lp} \times 10^{-7} \quad [mm] \text{ - - - (1)}$$

$$Lp = Ton \times \frac{Vin(AC)min \times \sqrt{2}}{Idp} \times 10^{3} \quad [mH] \text{ - - - (2)}$$

$$Idp = \frac{Ps \times 2 \times \sqrt{2}}{\eta \times Vin(AC)min} \quad [A] \text{ - - - (3)}$$

$$Ton = Don \times T\max = \frac{Don}{f\min} \quad [s] \text{ - - - (4)}$$

$$Don = \frac{Vo - Vin(AC)min \times \sqrt{2}}{Vo} \text{ - - - (5)}$$

where Ae is effective cross section area of core [mm^2], fmin is the minimum operating frequency [Hz] e.g. 40k-60kHz for universal input and 50-70kHz for single range input .

< turns of main winding Np >

Main winding turns Np is calculated from formula(6).

$$Np = Ton \times \frac{Vin(AC)min \times \sqrt{2}}{\Delta B \times Ae} \times 10^9 \quad [Turn] \quad \text{- - - (6)}$$

ΔB is core flux density [mT]. Generally less than 350mT is chosen to considering saturation under high temperature condition in general high frequency use ferrite material.

< turns of sensing winding Nc>

More than 1.5V is required as ZC winding pulse voltage in maximum input condition. So calculate turns of Nc winding from formula (7).

$$Nc > 1.5 \times \frac{Np}{Vo - \{\sqrt{2} \times Vin(AC)max\}} \quad [Turn] \quad \text{- - - (7)}$$

Np : Nc is almost 10 : 1 when assuming universal input Vin(AC)max is 264V and PFC output voltage Vo is 390V.

Example : Nc = 5 turns when Np = 50, Vin(AC)max=264V,Vo=390V (Nc>4.5).

< wire >

Np winding cross senction area is chosen considering rms current IL(rms) [A] and desired current density [A/mm^2] in specified condition.

Fig.34 shows IL(rms) versus output power example in AC 85V input condition.

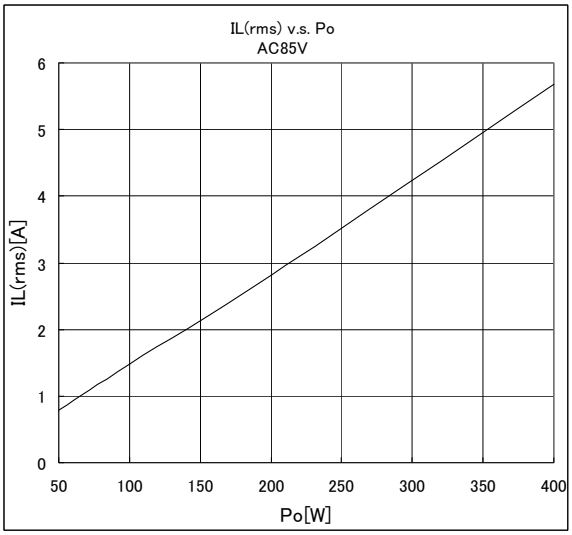


Fig.34 IL(rms) at AC 85V input

3.1.2 PFC MOSFET(Q141)

Rms current is calculated from formula (8)

$$I_{drain(rms)} = \frac{2\sqrt{2} \times P_{in}}{V_{in(ac)}} \times \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times V_{in(ac)}}{9 \times \pi \times V_o}} \quad \text{-------(8)}$$

Turn off current of MOSFET in CRM PFC is large, so take care of surge voltage at turn off instance. Generally Vds rating of > 1.2 x Vo is chosen.

3.1.3 PFC blocking (output) diode (D111)

Rms current is calculated from formula (9)

$$I_{Diode(rms)} = \frac{2\sqrt{2} \times P_{in}}{V_{in(ac)}} \times \sqrt{\frac{4\sqrt{2} \times V_{in(ac)}}{9 \times \pi \times V_o}} \quad \text{-------(9)}$$

Avalanche ruggedness of D111 cannot be expected, so voltage rating should be strictly considered. 600V FRD of low Vf type is recommended. CRM PFC does not require ultra-fast FRD, Vf is important. Please notice inrush current withstanding Ifsm when additional inrush bypass diode is not used.

Recommended diode example : D2(3)FK60 / S3K60 / SF3(5,8,10,20)K60M (Shindengen)

3.1.4 Inrush current bypass diode (D110) : optional

Inrush current bypass diode is used when PFC inductor audible noise at startup transient is not negligible or PFC blocking (output) diode rush current Ifsm withstand is poor. In this case choose general diode with enough Ifsm withstanding , not FRD.

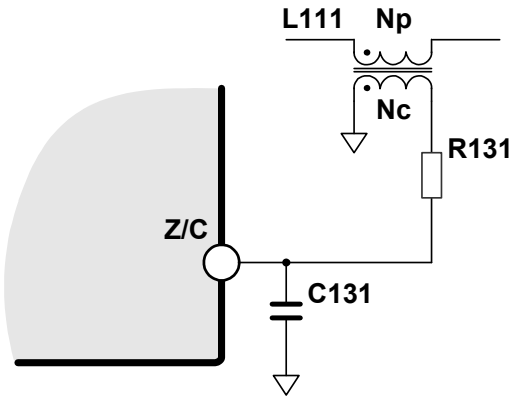
Recommended diode example : S2V60 / S3V60 / D3F60 / D4F60 (Shindengen)

3.1.5 ZC terminal

VGP turn on timing can be adjusted adding C131 between ZC and GND as shown in Fig.35. C131 delays turn on timing to switch at bottom of Vds swing valley. Initial value is open. Permissible terminal current of ZC terminal is +/-5mA, so limit terminal current to 80% rating by resistor R131 .

Rzc value should be larger than maximum value calculated from formula (10) and (11)

.



♦ Nc winding pulse voltage positive side

$$R_{ZC+} = \frac{Vo \times \left(\frac{Nc}{Np}\right) - 7.5}{4 \times 10^{-3}} \quad [\Omega] \quad \text{- - - (10)}$$

- 7.5V is ZC terminal clamping internal zenor voltage

♦ Nc winding pulse voltage negative side

$$R_{ZC-} = \frac{\left(-Vin(AC)max \times \sqrt{2}\right) \times \left(\frac{Nc}{Np}\right)}{-4 \times 10^{-3}} \quad [\Omega] \text{- - - (11)}$$

Fig.35 . ZC connection

Design example of Vo=400[V], Vin(AC)max=276[V], Np=50[Turn], Nc=5[Turn] :

♦ Nc winding positive pulse voltage : $R_{ZC}+ = \dfrac{400 \times \left(\dfrac{5}{50}\right) - 7.5}{4 \times 10^{-3}} = 8.1[\mathrm{k}\Omega]$

♦ Nc winding negative pulse voltage : $R_{ZC}- = \dfrac{\left(-276 \times \sqrt{2}\right) \times \left(\dfrac{5}{50}\right)}{-4 \times 10^{-3}} = 9.8[\mathrm{k}\Omega]$

So ZC current limitting resistor R131should be larger than 9.8kΩ.

3.1.6 Phase compensation (R132,C132,C133)

Error amp is a transconductance amp (gm amp). Connect C/R filters for phase conpensation as described in Fig.36.

C133 value is calculated from formula(12). Choose around 20Hz for cut off frequency fc . C132 ≈ 1/10 x C133.

$$C133 \approx \frac{130}{2\pi \times fc} \quad [\mu F] \quad \text{- - - (12)}$$

- gm amp transconductance is 130 [μA / V]

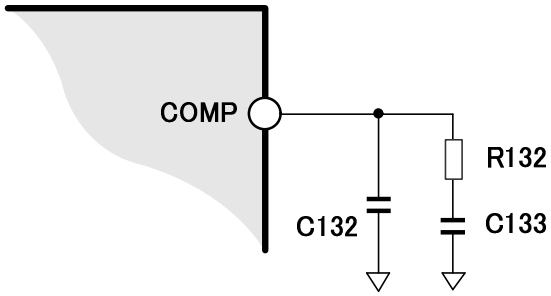


Fig.36 . COMP terminal connection

Transconductance of gm amp is 200[μA/V] when SST terminal voltage is less than 1.5V.So PFC output overshoot and undershoot is suppressed at startup period.

Although larger R132 increases gain in higher frequency region than fc, too large R132 causes waveform distortion. Start with 1k – 10kΩ as initial value.
Recommended initial value example : R132=1kΩ,C132=0.22μF,C133=2.2μF

Adjust C/R values in actual operation.

3.1.7 PFC output voltage adjustment (R111～R115,C112)

PFC output voltage is sensed by voltage divider（R111 - R115）and applied to FBP terminal as shown in Fig.37.
Error amp threshold voltage is 3.0V, so dividing ration is calculated from formula (13).R111-114 is considerably high inpedance to supress ineffective power loss.3 – 4MΩ is recommended when assuming PFC output voltage is around 400V.
Add filtering capacitor C112 of 1000pF – 2200pF in paralleled to FBP and GND.

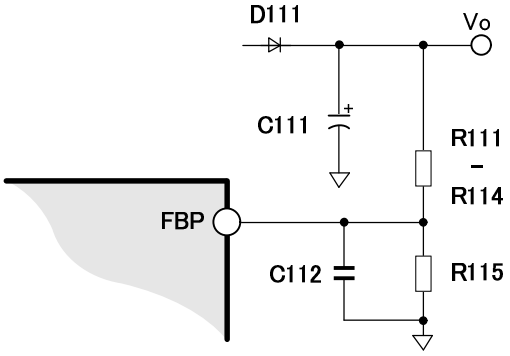


Fig.37 . FBP connection

$$(R111+R112+R113+R114)=\frac{R115\times(Vo-3.0)}{3.0}\quad[\Omega]\text{ - - - (13)}$$

Please take notice about tolerance and temperature coefficient of high voltage sensing resistor.
And also electrolytic corrosion is sensitive in high voltage sensing use, cheap carbon-film resistor is not recommended.

3.1.8 PFC OCP operation point adjustment (R121,R126,C121)

Cycle by cycle current limitting point is determined by R121 value in formula (14).

Choose desired maimum limitting output power Ps as 1.2 – 1.5 x Pomax.
Take notice about flux density in worst case considering core saturation.
Generally insert RC filter for sensing voltage smoothing, 1000pF for C121 and 100-1kΩ for R126.

$$R121=0.5\times\frac{\eta\times Vin(AC)min}{2\times\sqrt{2}\times Ps}\quad[\Omega]\text{ - - - }\quad(14)$$

3.1.9 PFC output capacitor selection (C111)

Dynamic OVP(over voltage protection) operating threshold is 1.08 x Vth (3.0V).
So consider voltage rating with enough margins .

$$Vo(OVP)=Vo\times1.08\quad[V]\quad\text{- - - (15)}$$

Please notice ripple current flows in output capacitor C111 has two element,and its rms current is expressed as formula (38) in worst case.
(LLC and PFC operating frequency and phase is independent)

$$I_{Co(rms)}=\sqrt{(I_{PFC})^2+(I_{LLC})^2-I_o{}^2}\qquad\text{------ (38)}$$

where IPFC equals to PFC diode rms current described in section 3.1.3 and ILLC is almost same as LLC high side MOSFET drain current described in formula (39) of section 3.2.2.

3.2 LLC section

3.2.1 LLC main transformer

LLC works well in resonant point operation (CRM) considering efficiency and EMI
Hereinafter LLC is assumed to operate in CRM.
FHA (fundamental harmonics approximation) analysis using inductance ratio and Quality factor Q based design posibbly cannot optimise resonant condition.
In this section general parameter selection using actual value is described.

(1) choosing Inductance and capacitor value
(2) choosing turns ratio
(3) flux density confirmation
(4) final study in actual operation

(1) choosing Inductance and capacitor value

Table 21 shows typical Cr value according to output power and input voltage spec when nominal operating frequency is from 50kHz to 100kHz.

Table .21 typical resonant capacitor value

Output power	AC100V	AC200V	PFC(DC390V)
50W - 100W	0.10uF	0.027uF	0.010uF
100W - 200W	0.15uF	0.033uF	0.022uF
200W - 300W	0.22uF	0.047uF	0.033uF

Calculate Lp setting frequency to 0.75 x fr (resonant frequency) by formula (16)

$$f \times 0.75 = \frac{1}{2 \times \pi \sqrt{(Lp \times Cr)}} \quad \text{- - - (16)}$$

Lr and Lp inductance ratio is important, in this case 20% - 30% of Lp is assumed as Lr.
Leakage inductance (= resonant inductance) is depende on transformer bobbin and winding structure, inductance adjustment is necessarry after final transformer is fixed.

Main resonant frequency **fr** is expressed as formula (17)

$$fr = \frac{1}{2 \times \pi \sqrt{(Lr \times Cr)}} \quad \text{- - - (17)}$$

(2) Turns ratio

Turns ration (n=Np/Ns) determines CRM point (Input dc voltage where LLC works in CRM operation).

$$n = \frac{Vin}{2 \times k \times (Vo + VF)} \quad \text{- - - (18)}$$

k : coupling coefficient
equivalent turns ratio neq=k×n
VF : output diode forward voltage

coupling coefficient **k** is expressed as formula (19)

$$k = \sqrt{1 - \frac{Lr}{Lp}} \qquad \text{- - - (19)}$$

Lp : primary inductance
Lr : leakage inductance (= resonant inductance)

Primary main winding turns Np is expressed as formula (20) using AL-value(AL).

$$Np = \sqrt{\frac{Lp}{AL}} \qquad \text{- - - (20)}$$

AL : AL-Value

$$Ns = \frac{Np}{n} \qquad \text{- - - (21)}$$

Circuit simulation study using parameters calculated above is recommended..

(3) flux density

Confirm magnetizing flux density ΔBm.

$$\Delta Bm = \frac{L_p \times I_{pk}}{N_p \times A_e} \qquad \text{- - - (22)}$$

Magnetizing current peak in CRM operation is expressed as formula (23)

$$Ipk(Lm) = \frac{Vo \times neq}{4 \times Lm \times fr} \qquad \text{- - - (23)}$$

(4) Study by actual operation

Exam following items in actual operation.

- Supressing of Startup didt occurance.
- Capacitive mode margin in power off holdup period and OCP operating condition.
- Stable switching under dynamic load condition
- VB voltage increase in OCP1 operation at shorted load condition
- FBL waveform stability
- Vds rating of PFC and LLC during shorted load condition
- Gate – source voltage turn off ringing of PFC and LLC

3.2.2 LLC MOSFET (Q241,Q242)

LLC MOFET drain current in ideal CRM operation is calculated from formula (39), MOSFET loss can be simply estimated as Rds x Idrain(rms)^2 as initial value.

$$I_{drain(rms)} = \sqrt{\left(\frac{\pi \times I_o}{4 \times n_{eq}}\right)^2 + \left(\frac{V_o \times n_{eq}}{8 \times L_m \times f_r}\right)^2} \qquad \text{-------- (39)}$$

where : Io = output dc current, Vo = output voltage , neq = equivalent turns ratio
Lm = magnetizing inductance , fr = resonant frequency of Cr and Lr

Vo x 1.2- 1.3 is enough as voltage rating of LLC MOSFET because Vds is clamped to input dc bus voltage (= PFC output voltage.).Vds surge voltage of turn off instance caused by parasitic inductance becomes maximum at OCP1 operating condition.

3.2.3 LLC oscillator (C211,R211,R212)

LLC operation control is performed by varying Ct discharging current. (Fig.38)
LLC Gate drive dead time , start frequency (fss) , Minimum frequency (fmin) and maximum frequency (fmax) is determined by Rt , Ct and R212 shown in Fig.38.

Ct : timing capacitor
Rt : timing resistor
FB : fmax adjusting resistor

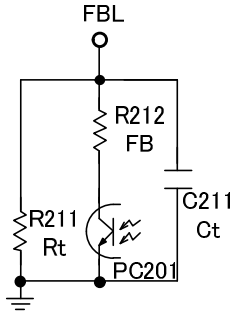


Fig. 38. FBL terminal connection

3.2.3.1 Dead time and initial startup frequency fss

Initial dead timer is determined by Ct and Rt as shown in Fig.39.
Dead time is not constant and it increases according to operating frequeny increases. This characteristics helps to keep ZVS in wide LLC operation range.

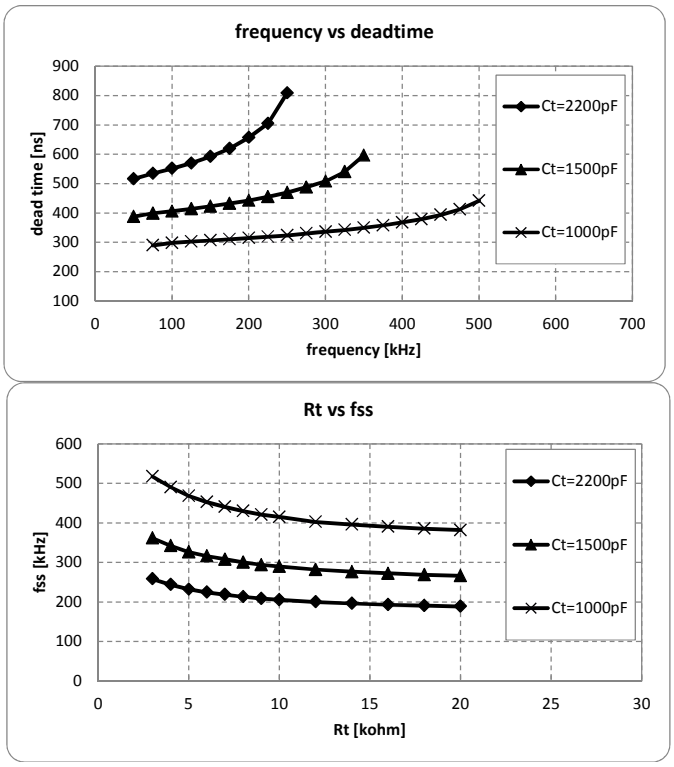


Fig.39. dead time and fss

3.2.3.2 Minimum frequency (fmin)

Minimum frequency (fmin) is determined by timing capacitor Ct and timing resistor Rt. Fid.40 shows the characteristics of frequency vs Rt and Ct value.

Basically Ct charging time (= dead time) and discharging time (ON period) is calculated from formula (24) and (25) ,

Minimum frequency fmin is expressed as formula (26).

Vfbl(top) and Vfbl(bottom)1 is varied slightly in actual operation due to internal delay time.

Please refer to precise design calculation sheet supplied to the customers separately .

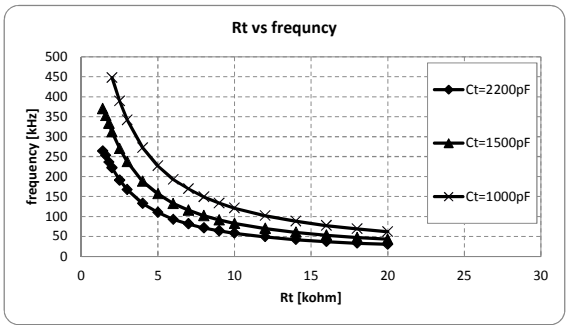


Fig.40. Rt vs frequency

$$t_{charge} = \frac{Rt \times Ct \times Vfbl_{(top)}}{Rt \times 9.0 \times 10^{-3} - Vfbl_{(top)}} - \frac{Rt \times Ct \times Vfbl_{(bottom)1}}{Rt \times 9.0 \times 10^{-3} - Vfbl_{(bottom)1}} \quad \text{- - - (24)}$$

$$t_{discharge} = -Rt \times Ct \times \ln \frac{Vfbl_{(bottom)1}}{Vfbl_{(top)}} \quad \text{- - - (25)}$$

$$f_{min} = \frac{1}{2 \times \left(t_{charge} + t_{discharge}\right)} \quad \text{- - - (26)}$$

3.2.3.3 Maximum frequency (fmax)

Maximum frequency is determined by Ct and total resitance connected to FBL terminal. Total resiatance Rt1 is paralleled resiatance of Rt and FB when Vce of opto coppler PC201 is assumed as zero volt. So fmax is calculated from formula (24) – (26) substituting Rt1 to Rt.

$$Rt1 = \frac{Rt \times FB}{Rt + FB} \quad \text{- - -} \quad \textbf{(27)}$$

3.2.4 LLC soft start (C235)

In this section timer delayed protection timing during protection mode and starting time constant of startup period are described.

SST capacitor starts to be charged by 30uA constant current when SST terminal voltage exceeds 06V. OCP timer charging is enabled when SST terminal voltage exceeds 1.5V, so startup should be completed before SST terminal voltage reaches to 1.5V. Thus transient period to 1.5V is calculated as startup time tss.as formula (28). Refer to MCZ5209 spec sheet to see SST terminal voltage and operating frequency characteristics detail.

$$t_{ss} = \frac{0.9 \times C235}{30 \times 10^{-6}} \qquad \text{- - - (28)}$$

SST capacitor charging current during OCP1 operation and di/dt protection in active stdby mode Itimer(charge)1 is 40uA, so transit time until SSTvoltage reaches to 3.5V is calculated from formula (29).

$$t_{timer} = \frac{1.4 \times C235}{40 \times 10^{-6}} \qquad \text{- - - (29)}$$

SST charging current during OCP2 operation is varied according to CSO terminal voltage. の時の chargin current Itimer(charge)2 when CSO ≤1.5V is 1.7uA, so transit time until SST voltage reaches to 3.5V is cauculated from formula (30).

$$t_{timer} = \frac{1.4 \times C235}{1.7 \times 10^{-6}} \qquad \text{- - - (30)}$$

Timer charging current Itimer(charge)3 is 40uA when CSO terminal voltage is larger than 1.5V In this condition Ttimer where SST terminal voltage reaches to 3.5V is calculated from formula (29).

SST capacitor discharging current Itimer(discharge) after SST terminal voltage reached to 3.5V and gate outputs are disabled is 6.7uA. Gate outputs disable status is initialized when SST terminal voltage decreases to Vtimer(reset) of 0.3V. Thus converter operation halt time period Ttimer(stop) during OCP timer delayed protection is calculated from formula (31).

$$t_{timer(stop)} = \frac{3.2 \times C235}{6.7 \times 10^{-6}} \qquad \text{- - - (31)}$$

In BURST mode, SSC terminal internal sinking is disabled so timing capacitance equals to total capacitance of C235 and 236 connected in series, it is expressed as formula (32).

$$C(ser) = \frac{C235 \times C236}{C235 + C236} \qquad \text{- - - (32)}$$

Substitute C235 to C(ser) in formula (28) – (31) when burst mode is assumed.

3.2.5 OCP operation point adjustment (R221,R225,R226,C222)

CSL terminal is the sensing input of main resonant current. MCZ5209 can be applied to both of resistor sensing method and capacitor sensing method.

Resistor sensing is inexpensive and sensing deviation is small but sensing resistor produces small loss of 0.2 – 0.3W.

Capacitor sensing loss is smaller than resistor sensing, but sensing deviation is large.

Resistor sensing connection example is shown in Fig.41.

10 - 47Ω is recomended for CSL filtering and adjusting resistor R255. Please consider CSL sourcing current of 90uA. R226 is for sensing voltage adjustment. Add filering capacitor C222, around 0.01uF is recommended.

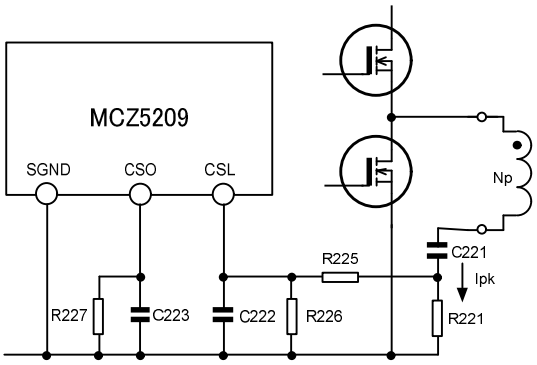


Fig.41. CSL/CSO connection

Sensing resistor R221 value is calculated from formula (33), where Ipk is desired resonant current peak when OCP2 operation starts. Opetaing point can be adjusted using sensinde voltage divider of R225 and R226. Calculate R226 using 10Ω - 47Ω as ,R225 from formula (34).

After actual resiator value is fixed, recalculate Ipk using formula (35).

$$R221 > \frac{0.35}{Ipk} \quad [ohm] \quad \cdots(33)$$

$$R226 = \frac{0.35 \times R225}{Ipk \times R221 - 0.35} \quad [ohm] \quad \cdots(34)$$

$$I_d = \frac{R225 + R226}{R226 \times R221} \times 0.35 \quad [A] \quad \cdots(35)$$

Add C223 and R227 to CSL terminal. C223 is charged when OCP1 or OCP2 operates and operating frequency increases according to CSO terminal voltage.
Frequency characteristocs is shown in table 13. Adjust C223 in actual operation.
For example long interval as 5 second latching is possible using large C223 capacitance like In audip amp aplication usage.
As intial value, choose 0.1uF – 1uF for C223 and 10k – 100k for R227.

3.3 Common part

3.3.1 Self bias winding

When using HV startup , generally LLC bias winding output voltage is used as self bias Vc1 voltage. After Vc1 supply is established, internal HV startup switch is disabled and produces no startup part power consumption. Bias winding voltage should be 12.6V in worst case condition including burst mode operation.

Fig.42 shows self-bias vcc circuit example.

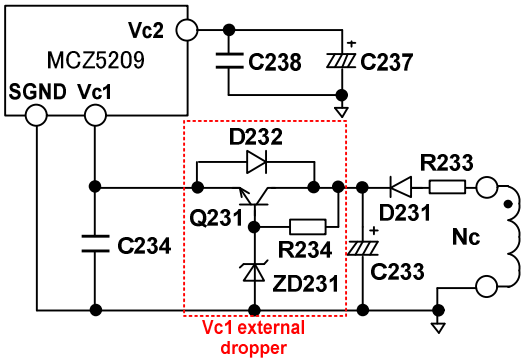


Fig.42 bias winding connection

Vc1 maximum rating is 35V. If winding output dc voltage exeeds 30V in worst condition, add external Vc1 dropper as shown in Fig.42. Winding output dc voltage is maximum at input bus voltage minimum and Po max or OCP operating condition when using loose coupled LLC transformer primary winding.
Also external vcc dropper reduces MCZ5209 temperature rise.
Output voltage of external vcc dropper should be larger rhan 12.6V in worst condition.
R233 is a few ohms to limit rush current and adjust winding output dc voltage.
D1FL20U M1FL20U D1NL20U (200V UFRD) or D1FJ10 (SBD) – Shindengen is recommended for D231.

3.3.2 Line sensing

Half wave LS terminal connection example is shown in Fig.43.Rectified half wave voltage is devided and smoothed by R104-107 and C107 and applied to LS terminal. Sensing voltage time constant can be shortened by smaller C107 using full wave retification from both AC line.
LS terminal voltage in half wave sensing VLSin is calculated as formula (36). C107 value is chosen to keep sensing voltage ripple smaller than sensing threshold hysterisis. Too large C107 increases starup delay after AC input is applied.

Fig.43 shows an example of AC90V - AC264V input spec.,R104 - R107=2.2MΩ, R108=560kΩ, C1=0.47uF are chosen.R108, C107 should be placed close to MCZ5209SN LS terminal.

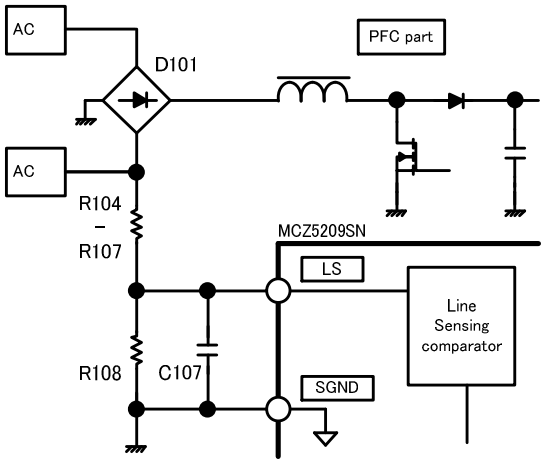


Fig.43. LS connection

LS terminal voltage at input voltage AC(rms) VLSin is :,

$$VLSin = \frac{AC(rms)}{1.72} \times \frac{R2}{R1+R2} \quad [V] \qquad \text{- - - (36)}$$

Sensing divider R1+R2 consumption is calculated by formula(37).

$$Rloss = \left(\frac{AC(rms)}{1.3}\right)^2 \div (R1+R2) \quad [W] \qquad \text{- - - (37)}$$

3.3.3 Burst mode and Active stdby mode selecting component value

Fig.44 shows an example of burst / active stdby selecting circuit configration with external signal. Secondary housekeeping output voltage during burst mode operation is assumed as 5V dropper output connected in output 12V line.

[BURST timing setting components]

15kΩ is chosen for R231 considering BURST terminal sinking current 400uA, and 75kΩ was chosen for R232 to satisfy BURST terminal voltage exceeds 2.0V when Vc1 is 12V (Vc1 UVLO) R255 determines sinking current from BURST terminal of output drop bottom limitting operation Worked. In this case 4.7kΩ is chosen as R255 to sink 400uA at BURST = 2.0V condition. Burst off period can be adjusted by C232, 0.01uF in this case.

[Output voltage drop bottom limitting components]

In open load or extremely ligh load, burst interval is simply determined by primary IC supply voltage Vc1 and output housekeeping voltage 5V is stabilized. But when 5V load is increased ,5V dropper input voltage (= 12V in this case) possible reaches to less than 5V because output voltage ripple decaying slope during burst operation is determined by 12V/5V output capacitance and 5V load resistance.
To avoid 5V output voltage drop, bottom keeping function is added as in Fig.44. Bottom minimum is set to 6.2V. Reference voltage of shunt regulator IC302 (2.5V) and output voltage sensing divider R384 and R385 determines output bottom voltage limit. More than 1mA is recommended as collector current of Q301 when Q301 turn ons.
When open load consumtion is sensitive during burst mode, use low current shunt regulator IC as IC302 and increase R383 value.

[ASTBY terminal voltage setting components]

Dividing voltage by R256 and R257 is applied to ASTBY terminal when Active stdby signal is low. 3.2V to 4.0V is necessary to keep IC operation in Active stdby mode.Please consider Q251 Vce(sat) and D251 Vf.

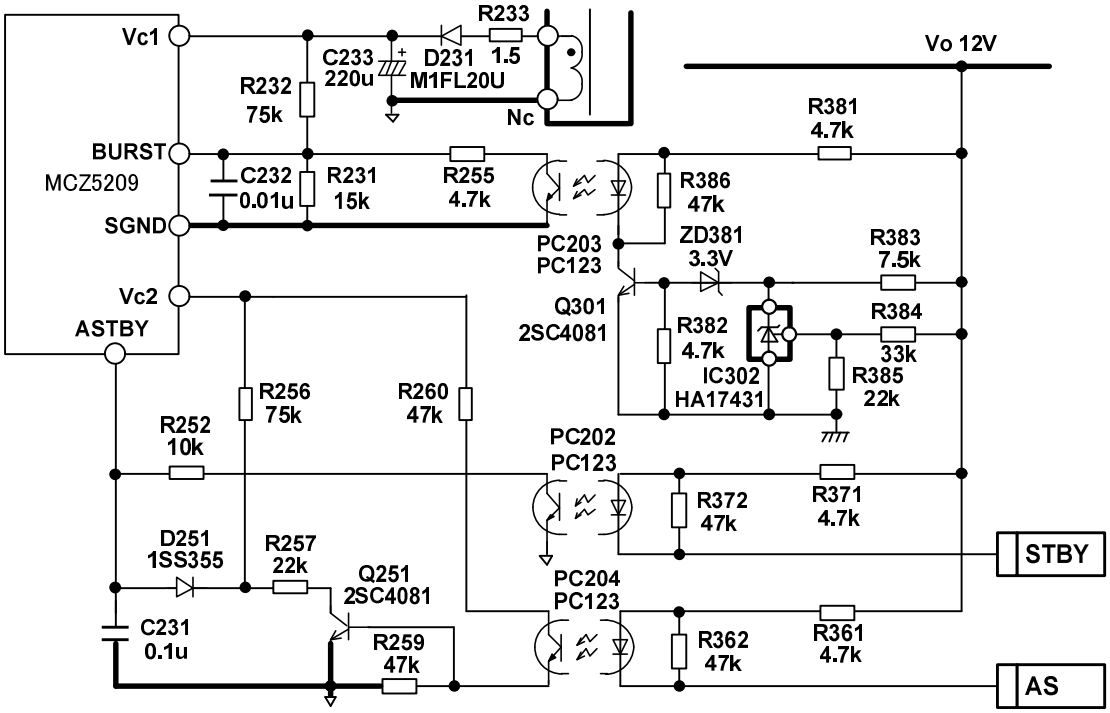


Fig.44. Additional circuit example for Burst / Active stdby

4 . Application example

4.1 Single output self-bias LLC

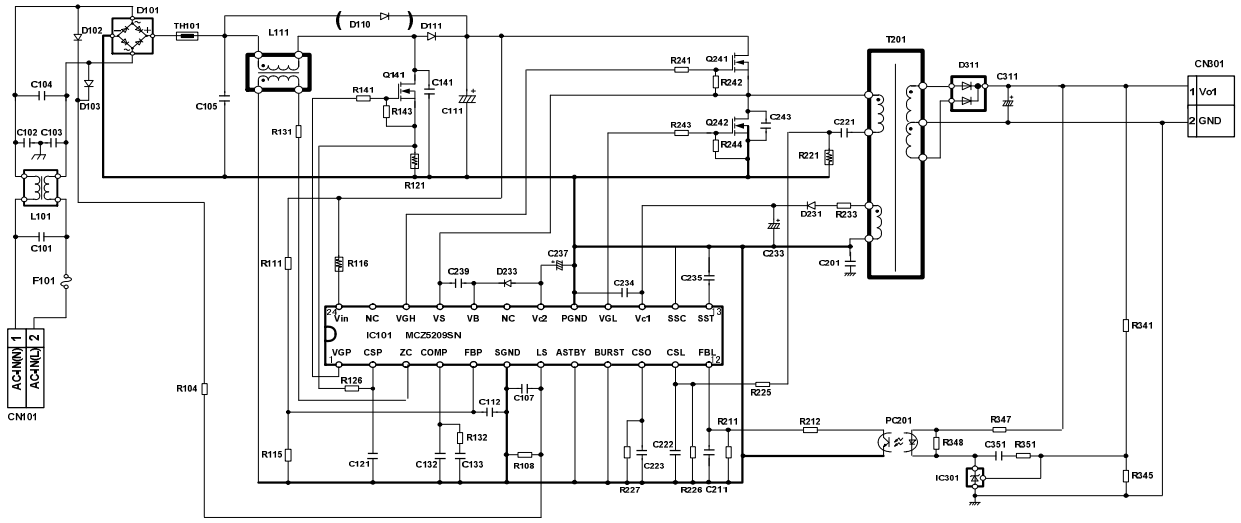
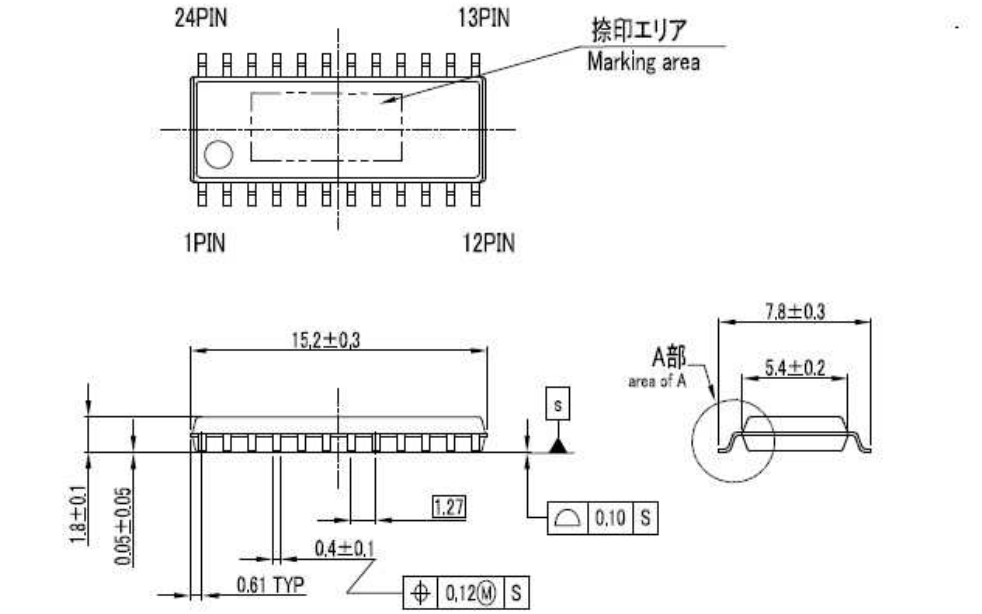
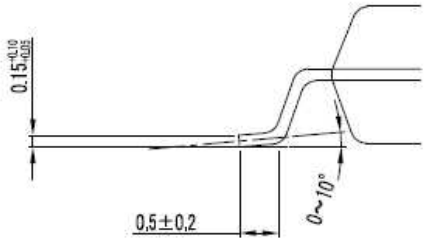


Fig. 45. Typical application circuit

5 Mechanical dimension

5.1 SOP24





A部詳細図
Detail area of A

製品重量：0.*g（標準）
Package weight：0.*g（TYP）

Notes: