CAT.No.1A0703-1E

LED Driver
Control IC

MV2002SG
MV2052SG

Application Note
Version 2.0

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WARNING		Indicates hazards that may lead to death, serious injury, or serious damage to property if the product is handled improperly.
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Contents

1. Overview

1.1 Features

The MV2002SG and MV2052SG are two-channel LED driver ICs that can be configured using just low-voltage pins via an external power supply.

One control IC is used to control the current for two channels, providing excellent relative current accuracy and enabling consistent color reproduction.

Current critical control is possible through quasi-resonant operation without auxiliary windings, enabling high efficiency and low noise using a simple power supply configuration.

With conventional current critical control, the switching frequency increases as the dimming rate decreases, resulting in drawbacks such as increased switching losses and limitations on minimum dimming values. The MV2002SG and MV2052SG, however, automatically switch from current critical operation to current discontinuous operation with the decrease in dimming rate, and this suppresses the increase in switching frequency, reducing switching losses and enabling smooth flicker-free deep dimming.

Oscillation on/off control is also possible by adjusting the RC pin voltage or dimming pin voltage (REF1, REF2) above or below a threshold voltage.

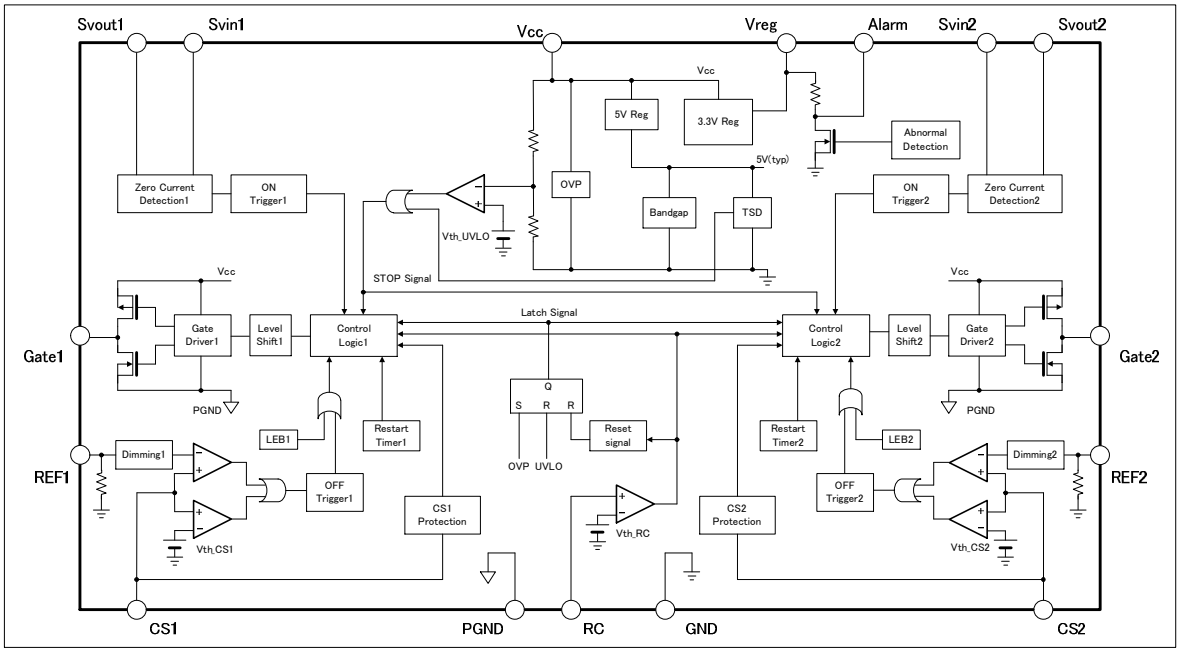
The ICs incorporate a power supply for an external microprocessor to supply a microprocessor voltage without three-pin regulators or similar devices.
(MV2002SG: 3.3 V, MV2052SG: 5 V)

The main features of the MV2002SG/MV2052SG are as follows:

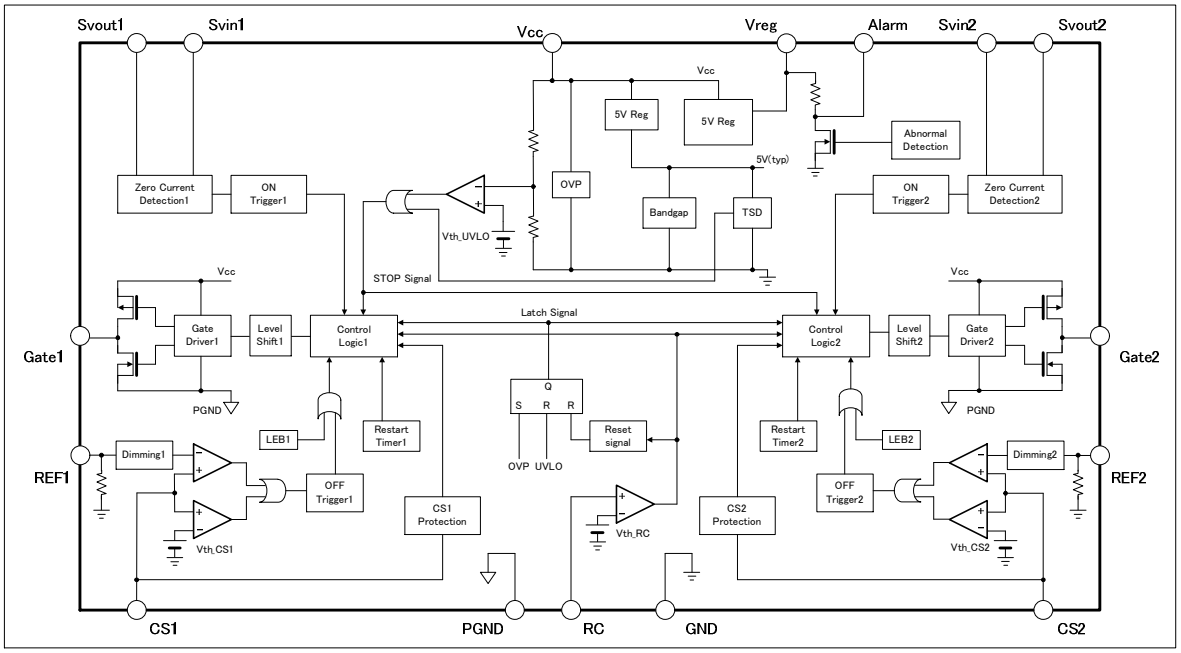
- Excellent relative current accuracy for each channel provides consistent color temperature when dimming.
- Allows quasi-resonant operation without auxiliary windings.
- Quasi-resonant operation using current critical control provides high efficiency and low noise with minimal input fluctuation.
- Allows deep dimming using off-time modulation (not exceeding 1 %).
- Allows PWM dimming and linear dimming.
- Allows oscillation on/off control using the RC pin and dimming pin (REF1, REF2).
  (Oscillation starts when V_{RC} > Vth_RC_st and V_{REF} > Vth_REF_st.)
- Incorporates built-in power supply for external microprocessor (3.3 V for MV2002SG, 5 V for MV2052SG).
- Outputs an alarm signal on detecting abnormal operation.
- Allows LED open protection using the auxiliary windings.
- Incorporates overheat protection and UVLO/LED short-circuit protection functions.
- Allows configuration using only low-voltage pins via use of external startup circuit.

1.2 Block diagrams

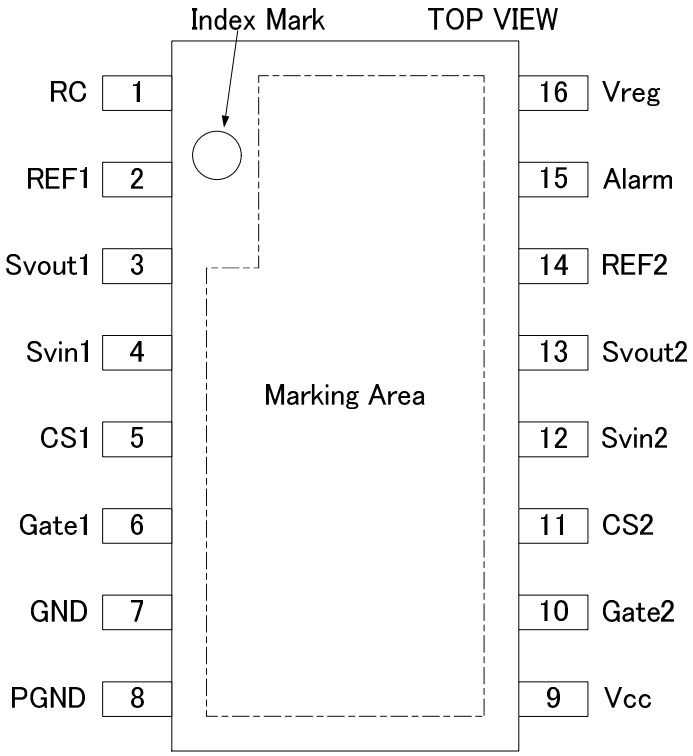
● MV2002SG



● MV2052SG



1.3 Pin assignment diagram



Package : SOP16

1.4 Pin function list

Pin No.	Symbol	Name
1	RC	Remote control pin
2	REF1	Channel 1 dimming pin
3	Svout1	Channel 1 zero current detection pin
4	Svin1	Channel 1 zero current reference pin
5	CS1	Channel 1 current detection pin
6	Gate1	Channel 1 MOSFET drive pin
7	GND	Ground pin
8	PGND	Power ground pin

Pin No.	Symbol	Name
9	Vcc	IC power supply pin
10	Gate2	Channel 2 MOSFET drive pin
11	CS2	Channel 2 current detection pin
12	Svin2	Channel 2 zero current reference pin
13	Svout2	Channel 2 zero current detection pin
14	REF2	Channel 2 dimming pin
15	Alarm	Alarm output pin
16	Vreg	External power supply pin

2. Basic Operations

The MV2002SG and MV2052SG are current-critical step-down chopper control ICs, with a circuit configuration as shown in Figure 1. In Figure 2, waveforms for the current flowing through the MOSFET and diode are represented by Id and I_F, respectively. In typical current-critical step-down chopper circuits, the MOSFET turns on after I_F becomes zero. This results in minimal diode recovery current, leading to lower losses and noise compared to PWM circuits. One downside, however, is that the oscillation frequency changes significantly with variations in output current (LED current), resulting in poorer dimming characteristics and efficiency.

The MV2002SG and MV2052SG detect Id, converted to a voltage, via the current detection pin (CS pin). On reaching the CS reference voltage, the MOSFET is turned off (peak current detection). The ICs perform current critical control by detecting when the diode current I_F becomes zero and the Svout voltage falls below the Svin voltage (zero current detection), turning the MOSFET on. The voltages at both ends of the choke (① and ② in Figure 2) are divided using resistors and input to the Svin and Svout pins to achieve current critical control without auxiliary windings. Additionally, the off-time modulation function keeps the frequency from increasing during dimming to ensure consistent efficiency and dimming characteristics even during deep dimming. (Refer to “5. Dimming Characteristics” on page 24.)

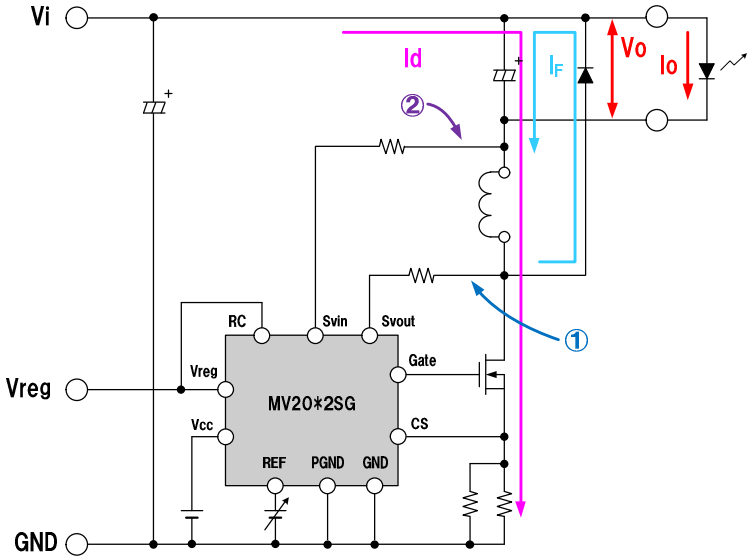
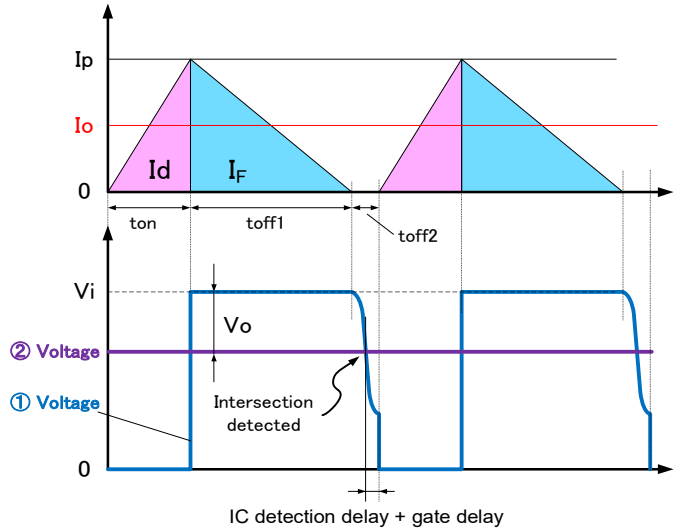


Figure 1 Current critical step-down chopper circuit



$$ton = \frac{L}{(Vi - Vo)} \times Ip$$

$$toff1 = \frac{L}{(Vo + V_F)} \times Ip$$

Figure 2 MOSFET and diode current waveforms for a current critical step-down chopper and voltage waveforms at both ends of the choke

2.1 Startup sequence

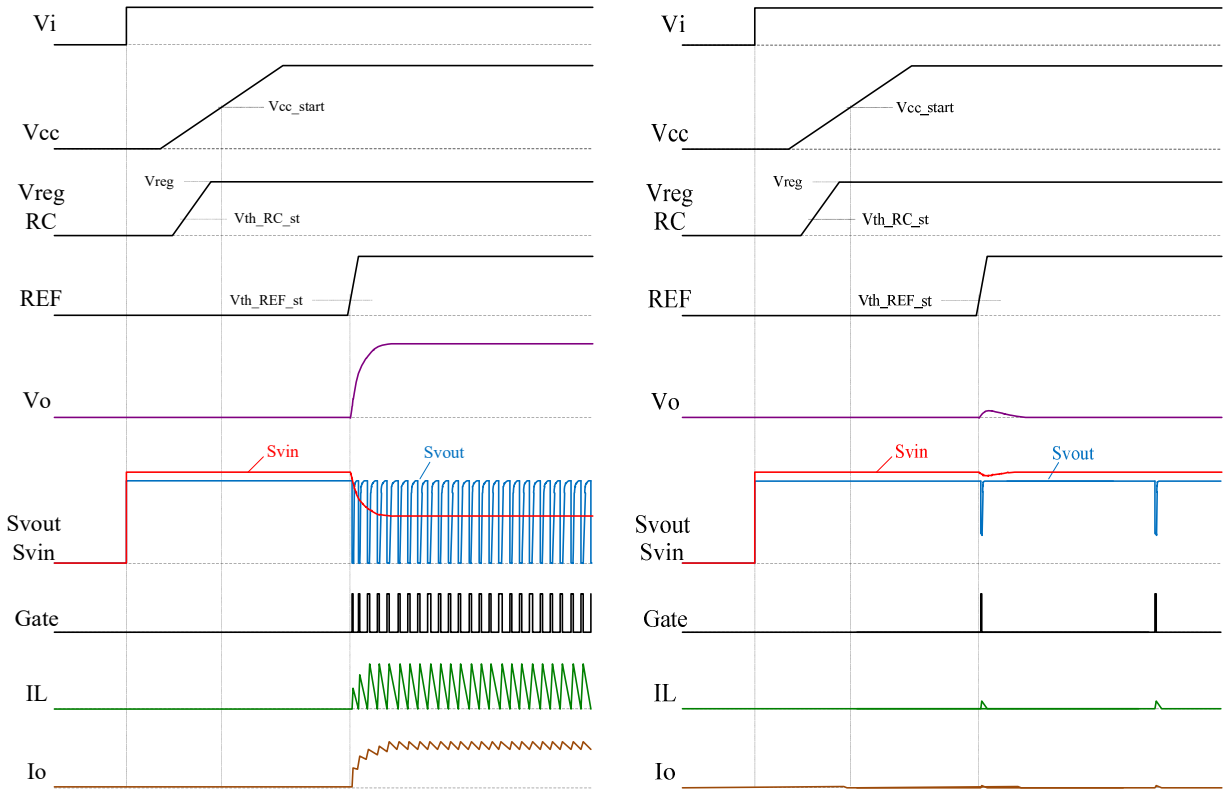
The MV2002SG and MV2052SG internal logic circuits start up when a voltage equal to or exceeding the starting voltage (Vcc_start) is supplied to the Vcc pin from an external power supply. To ensure stable operation, the signal should ideally be applied to the REF pin when the Vcc voltage is equal to or greater than the Vcc_start voltage. Note that the microprocessor power supply Vreg voltage outputs the preset voltage (3.3 V for MV2002SG, 5 V for MV2052SG) when the Vcc voltage is supplied.

Figure 3 shows startup sequence examples for the circuit configuration shown in Figure 1.

In the normal startup operation, oscillation starts when the RC pin voltage V_{RC} is equal to or exceeds the oscillation start RC pin threshold voltage (Vth_RC_st), the Vcc voltage is equal to or exceeds Vcc_start, and V_{REF} is equal to or exceeds the oscillation start REF pin threshold voltage (Vth_REF_st). Once oscillation starts, as the output voltage rises, the Svin voltage intersects the Svout voltage, enabling zero current detection. (Figure 3 (a) Successful startup operation)

In situations where charging the output capacitor is difficult—for example, when the gate resistor R13 (R23) has a high resistance or when the dummy resistor connected in parallel with the LED has a low resistance, the output voltage may not rise after oscillation begins, and zero current detection may not be possible. If zero current detection is not possible, the IC forcibly switches over to the restart operation using the minimum on-time and restart time instead of the normal peak current detection. The restart operation continues until zero current detection is possible. Thus, startup is not achieved unless the output voltage increases during the restart operation. (Figure 3 (b) Failed startup operation)

Be sure to measure the Svin and Svout voltages at startup on the actual apparatus to confirm that zero current detection has been achieved.



(a) Successful startup operation (b) Failed startup operation

Figure 3 Startup sequence examples

2.2 Regulator function

The MV2002SG and MV2052SG incorporate a built-in regulator power supply circuit that can be used for external circuits such as microprocessors. The regulator voltage Vreg is output as a preset voltage when the Vcc voltage is applied (3.3 V for MV2002SG, 5 V for MV2052SG). The internal regulator circuit includes drooping-type overcurrent protection, which lowers the regulator voltage when the regulator load current Ireg exceeds the drooping point. Figure 4 shows typical regulator characteristics.

When the regulator voltage falls below the voltage corresponding to the operation start voltage minus the hysteresis voltage (Vreg_start – Vreg_hys), the Gate 1 and Gate 2 oscillation is stopped. If Vreg rises back above the operation start voltage (Vreg_start), the gate oscillation is automatically restarted. During startup, an overly large capacitor should not be connected, to ensure that the Vreg voltage reaches Vreg_start before the Vcc voltage reaches Vcc_start. (Approximately 0.1 μF)

Note that even if gate oscillation is stopped by other functions, the regulator circuit will continue to operate, ensuring stable operation of the external circuits connected to the Vreg pin.

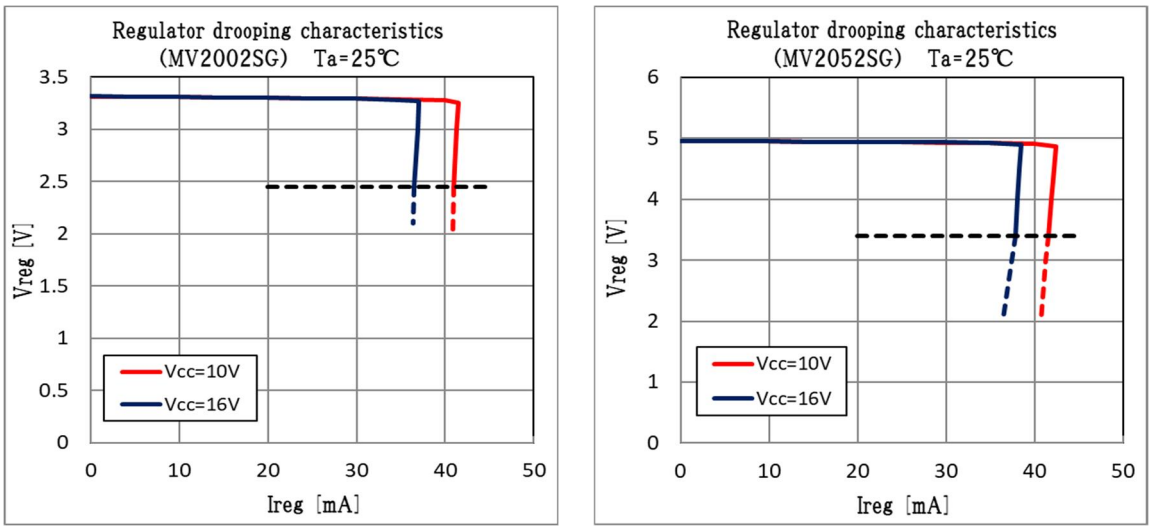


Figure 4 Typical regulator drooping characteristics

2.3 Remote control (RC) function

The MV2002SG and MV2052SG can simultaneously control gate oscillation on/off for two channels by applying an external signal to the RC pin. Oscillation is started by increasing the RC pin voltage V_{RC} above the oscillation start RC pin threshold voltage (Vth_RC_st), and is stopped by reducing the voltage below Vth_RC_st by the amount corresponding to the hysteresis voltage (Vth_RC_hys). Note that the regulator circuit continues to operate even when gate oscillation has been stopped by the RC function.

Since the RC pin is pulled down inside the IC, it should be connected to the Vreg pin, or an external voltage should be applied to start oscillation. If an external voltage is applied, take care to ensure that it does not exceed the absolute maximum rating of the RC pin.

V_{RC} can be applied again to release the latch stop due to the protective function. (For details of the protective function, refer to “2.4 Alarm signal output function.”)

When using remote control via the RC pin, connect a capacitor (approximately 1,000 pF) between the RC pin and GND pin to prevent noise-induced malfunctions.

2.4 Alarm signal output function

The MV2002SG and MV2052SG incorporate an alarm signal output function, which outputs a signal externally when abnormal operation is detected.

This function allows the other channel to be safely shut down when an abnormality occurs in one channel by responding to an alarm signal with a microprocessor or similar device.

The alarm signal is output on detection of Vcc_OVP or CS being open or when Ton_max occurs for 128 consecutive cycles (such as CS-GND being short-circuited). The voltage of the output alarm signal is the same as the Vreg voltage (3.3 V for MV2002SG, 5 V for MV2052SG). For details of the main abnormalities causing alarm signal output, refer to Table 1.

The alarm signal can be reset via the RC pin or Vcc pin. If the alarm signal is output due to Ton_max persisting for 128 cycles, the alarm signal will be automatically reset once Vcs reaches the reference voltage (peak current detection).

Note that the alarm signal will still be output even during startup or transient pauses in which the difference between the input and output voltages becomes small and Ton_max persists for 128 cycles. In situations like this where the alarm signal is output for only a limited duration, adjustment is required using control by microprocessors or other devices to ensure that there are no issues with the power supply.

Table 1 Alarm signal output for main abnormalities (abnormalities in channel 1)

Abnormal operation	Channel 1	Channel 2	Alarm signal	Reset method
Vcc_OVP	Oscillation stop (latch stop)		Yes	Vcc or RC reset
CS pin open-circuit	Oscillation stop (latch stop)	Normal operation	Yes	Vcc or RC reset
Short-circuit between CS and GND pins	Ton_max ⇔ Toff_max	Normal operation	Yes	Auto reset
LED short-circuit	Ton_min ⇔ Trestart	Normal operation	No	Auto reset
LED open-circuit (for basic circuit configuration)	Ton_max ⇔ Toff_max	Normal operation	Yes	Auto reset
TSD	Oscillation stop		No	Auto reset

3. Component Selection Procedure and Calculation Method

Calculations are approximate. In actual circuits, errors may occur for various reasons, including the characteristics of individual parts and IC detection delays. Check on the actual apparatus and make the necessary adjustments.

When using an oscilloscope to verify waveforms, note that the waveforms and characteristics will vary depending on probe capacitance. Pay close attention especially when measuring the Svin, Svout, and CS pins, and across D and S on the MOSFET.

Note that unless otherwise specified, the figures used in this document are typical values.

3.1 Basic circuit configuration

Figure 5 shows the basic circuit configuration for the MV2002SG and MV2052SG, and Figure 6 shows the operation waveforms.

The circuit in Figure 5 shows how detecting the voltages at both ends of the choke eliminates the need for auxiliary windings and enables a simple, low-cost circuit configuration.

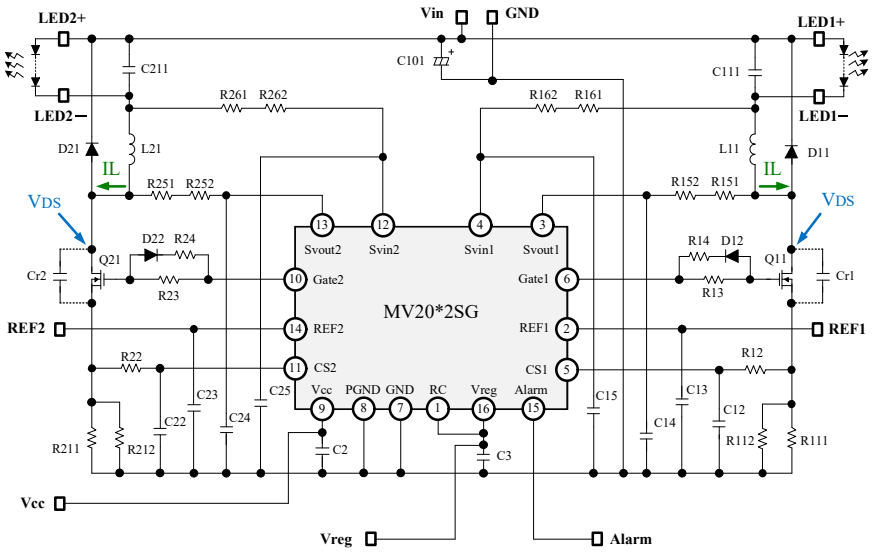
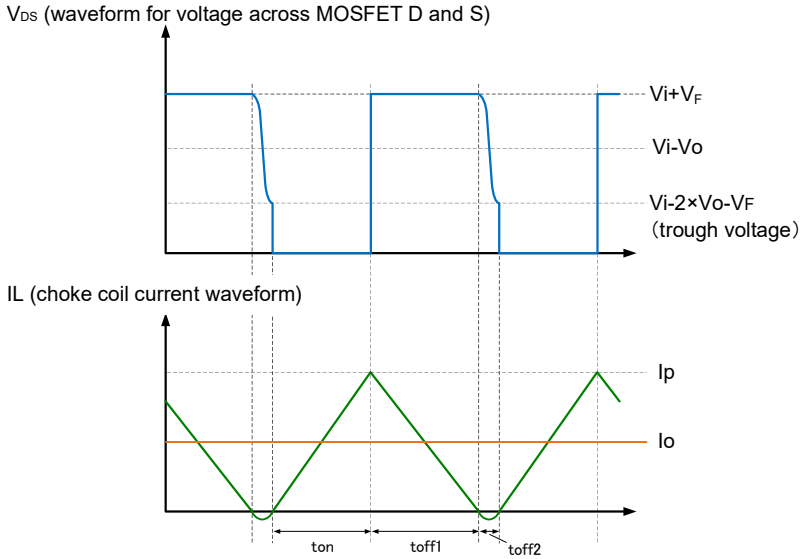


Figure 5 Basic circuit configuration



$$ton = \frac{L}{(Vi - Vo)} \times Ip$$

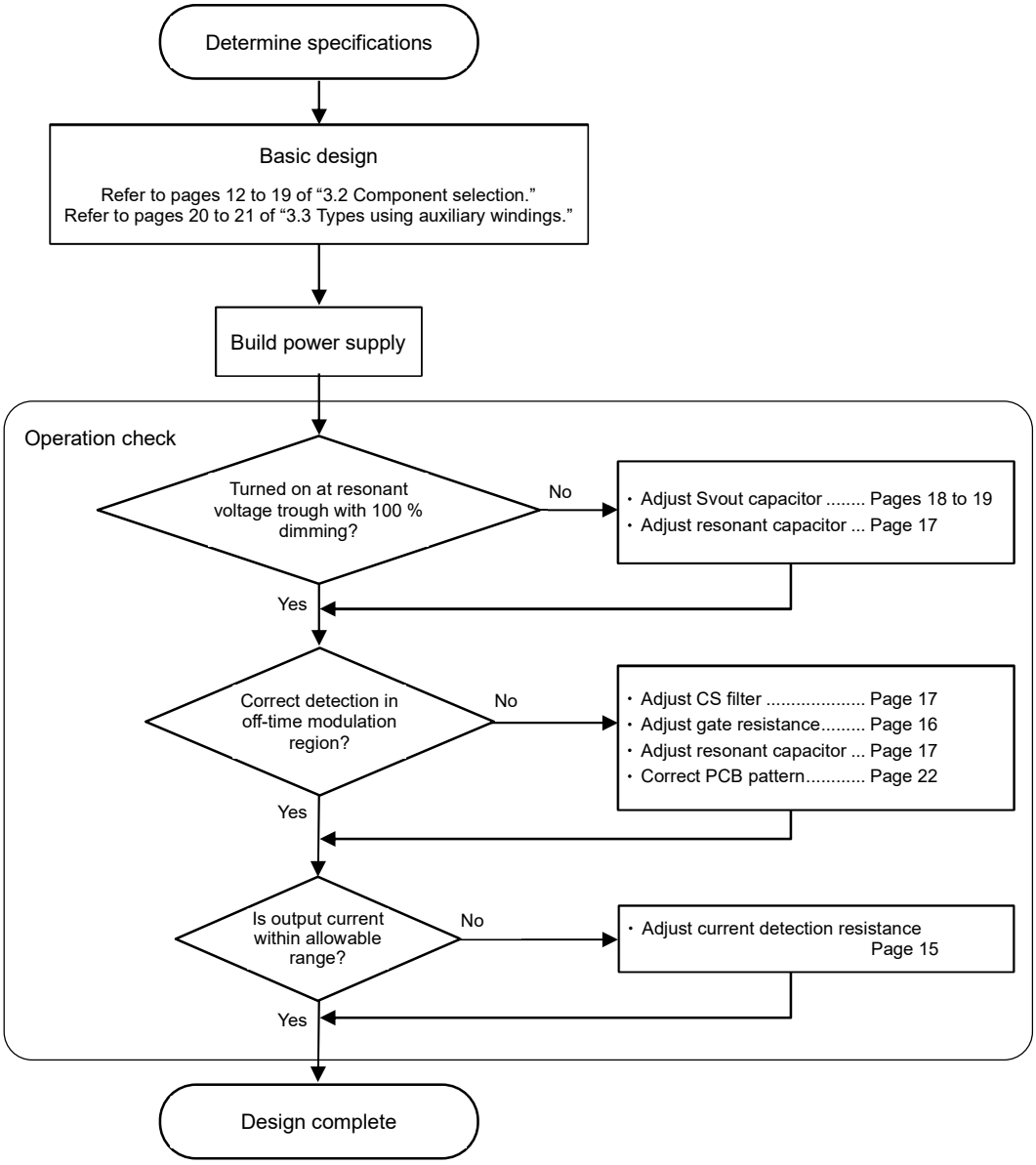
$$toff1 = \frac{L}{(Vo + V_F)} \times Ip$$

Figure 6 Basic operation waveforms

3.2 Component selection

The chart below shows the design procedure from determination of the specifications to adjustment. The design procedure provided here is one example of an electrical design process.

Undertake the design process in accordance with safety standards stipulated by official bodies and with your own company rules as necessary.



* The operation check must be repeated if any component constants are changed after the design has been completed.

・ Basic design precautions

Depending on factors such as PCB patterns, specifications, and peripheral constants, the internal voltage or thresholds may fluctuate immediately after the MOSFET turns off. As the MV2002SG and MV2052SG are two-channel drivers, threshold fluctuations in one channel due to MOSFET turn-off may affect the other channel. In such cases, the on/off detection points may shift, causing variations in the on-time, which may then cause fluctuations in the output current. When both channels operate at approximately the same switching frequency, on-time fluctuations are more likely to continue (synchronization), resulting in output current fluctuations in the range of several milliamps (mA). (Figure 7)

Effective ways to minimize output current fluctuations due to synchronization include implementing pattern design to suppress noise interference between channels and designing peripheral constants to reduce the synchronization period. More specifically, it is effective to offset the turn-off timing by designing the choke coil L value between channels 1 and 2 to create a difference of around 1:1.7 in the rated current switching frequencies (Figure 8) and by creating differences in REF ripple voltage (Figure 9).

When adjusting these constants, check the actual apparatus operation of characteristics such as the dimming characteristic switching points.

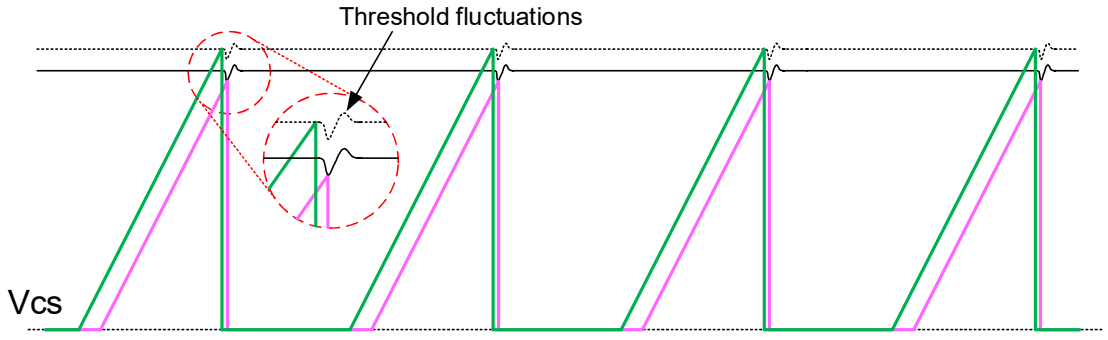


Figure 7 Schematic showing operation with synchronization

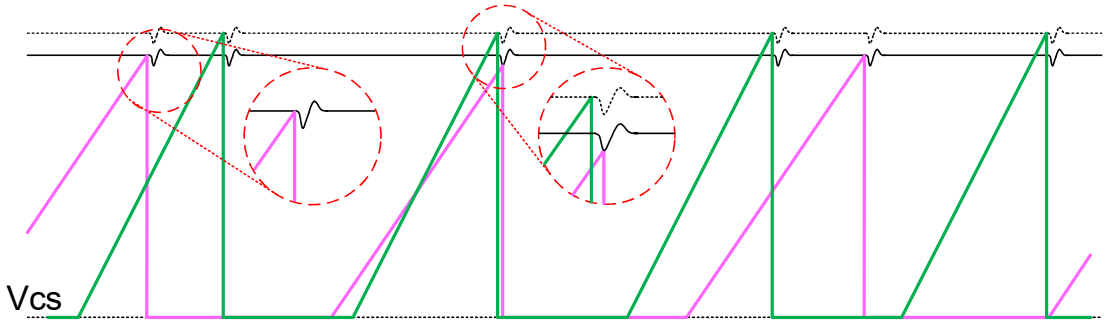


Figure 8 Schematic showing operation with difference in switching frequencies

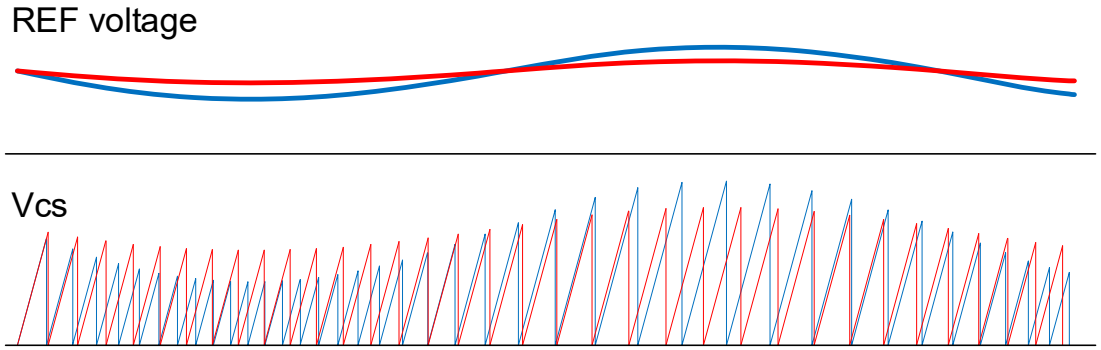


Figure 9 Schematic showing operation with difference in REF ripple voltage

3.2.1 MOSFET selection (Q11, Q21)

The MOSFET is subjected to the voltage V_{DS} shown in Figure 6. The maximum applied voltage approximately equals the maximum input voltage. In practice, voltage spikes may occur due, for example, to inductance (L) components of the wiring pattern. Check on the actual apparatus and select a component with sufficient withstand voltage.

MOSFETs with low on-resistance offer advantages in the case of lighting equipment with high power consumption, but with low power consumption lighting equipment, selecting MOSFETs with low Ciss and Coss capacitance will achieve higher efficiency and better dimming characteristics.

IC power consumption is the product of the input voltage and current consumption. Current consumption is the sum of the logic current and the gate drive current. Select MOSFETs with the lowest possible gate capacitance. (See Table 2 Recommended MOSFETs.)

Table 2 Recommended MOSFETs (as of March 2020)

Product name	Withstand voltage	ID(A)	Ron(typ)	Ron(max)	Qg(nC)	Ciss(pF)	Coss(pF)	Manufacturer	Package
P3B28HP2	280	3	1.7	2	3.6	120	25	Shindengen	FB
P6B28HP2		6	0.66	0.85	5.7	240	43	Shindengen	FB
P1R5B40HP2	400	1.5	4.2	5	3.9	120	20	Shindengen	FB
P4B40HP2		4	1.54	1.9	6.5	245	33	Shindengen	FB
P1B52HP2	525	1	6	7.2	4.3	125	20	Shindengen	FB
P5B52HP2		5	1.4	1.7	10.5	400	45	Shindengen	FB
P6B52HP2		6	1.1	1.35	15	520	58	Shindengen	FB
P0R5B60HP2	600	0.5	8.3	10	4.3	120	18	Shindengen	FB

3.2.2 Regenerative diode selection (D11, D21)

As with MOSFETs, regenerative diodes must have a withstand voltage greater than the input voltage. Select fast recovery diodes (FRD) suitable for high-speed switching with a trr value not exceeding approximately 100 ns. (Refer to Table 3 Recommended regenerative diodes.)

Table 3 Recommended regenerative diodes (as of March 2020)

Product name	Withstand voltage	Io(A)	V_F(V)	Cj(pF)	trr(ns)	Manufacturer	Package
D1FL20U	200	1.1	0.98	-	35	Shindengen	1F
D2FL20U		1.5	0.98	-	35	Shindengen	2F
D1FL40U	400	1.5	1.2	11	25	Shindengen	1F
D2FL40		1.3	1.3	-	50	Shindengen	2F
D1FK60	600	0.8	1.3	11	75	Shindengen	1F
D2FK60		1.5	1.3	16	75	Shindengen	2F

3.2.3 Current detection resistor selection (R111, R112 and R211, R212)

When the circuit is designed to achieve the rated current when V_{REF} is 2.7 V, the current detection threshold for the CS pin, Vth_CS_2_7, is set to 0.538 V, and R111//R112 (or R211//R212) = Rcs. In Figure 6, if toff2 is significantly shorter than ton or toff1, the Id peak current, Ip, is double the output current Io. Thus, Rcs is calculated as follows using Io (max), the output current for 100 % dimming:

$$Rcs = \frac{Vth\_CS\_2\_7}{Ip} = \frac{0.538}{2 \times Io(max)}$$

In practice, the actual current will vary slightly from the calculated value due to toff2 and detection delays. Adjust the resistance appropriately on the actual apparatus.

While implementing design to achieve the rated current when V_{REF} is 3.3 V or higher will not cause operational issues, it will reduce relative current accuracy.

3.2.4 Inductor selection (L11, L21)

Inductance is calculated as follows, where Vi is input voltage, Vo is output voltage (LED voltage), f is switching frequency, L is inductance, V_F is forward voltage drop of the regenerative diode, and toff2 is ignored:

$$L = \frac{(Vi - Vo) \times (Vo + V_F)}{2 \times f \times Io \times (Vi + V_F)}$$

The switching frequency varies with input voltage fluctuations and dimming.

Inductors typically have the DC superimposition characteristics shown in Figure 10 (a), with inductance decreasing as current increases. This results in the MOSFET current waveform indicated by the solid line in Figure 10 (b). The output current Io will be slightly lower than the calculated value.

The peak current Ip through the inductor will be approximately double the output current Io. Pay attention to the decrease in inductance at Ip when selecting the inductor.

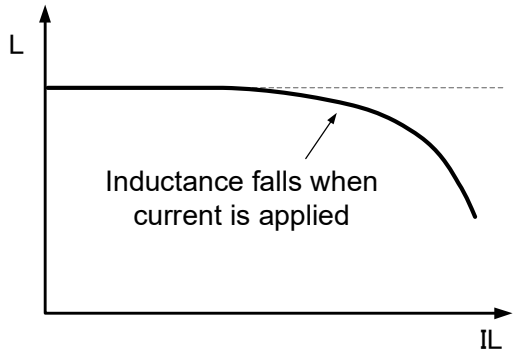


Figure 10 (a) Inductor DC superimposition characteristics

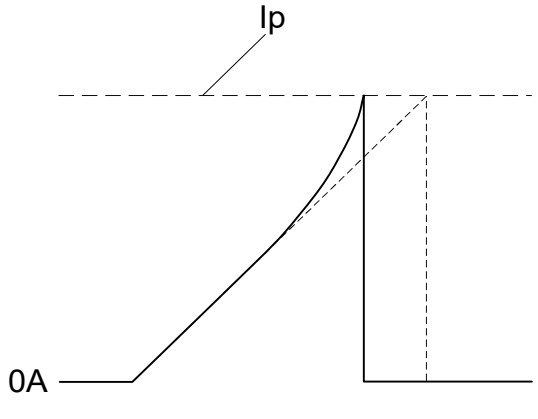


Figure 10 (b) MOSFET current waveform when inductance decreases

3.2.5 Gate drive circuit selection (R13, R14, D12 and R23, R24, D22)

The gate charging current (IG_source) inside the IC is limited to approximately 46 mA, and the discharge current (IG_sink) is limited to approximately 475 mA. This means the circuit can be used with R13 (R23) = 0 Ω, i.e., with a direct connection. Inserting R13 offers benefits such as delay adjustment, noise reduction, and improved dimming characteristics. However, if the resistance of R13 is too high, zero current detection may not be possible once the restart operation starts, possibly causing the restart operation to continue. When determining the resistance of R13, be sure to confirm that zero current detection is possible even after starting oscillation, by gradually increasing the REF voltage.

A discharge diode D12 (D22) and resistance R14 (R24) are also required to achieve good constant current characteristics without limiting the discharge current. The discharge current can be adjusted using R14.

Note that the charging current and discharge current above are values for Vcc = 10 V. They will vary depending on the Vcc value.

3.2.6 Svin and Svout pin resistance selection (R151, R152, R161, R162, and R251, R252, R261, R262)

The Svin and Svout pins are used for comparator input to detect voltage inversions at both ends of the inductor to determine the on-timing (zero current detection). To ensure effective comparator characteristics, the input voltage to the pins should not exceed 3.5 V. Both ends of the inductor are at high voltages, so voltage dividing resistors (R151 to R162) are required, as shown in the circuit diagram in Figure 11.

Due to the basic circuit configuration, an LED leakage current flows via the voltage dividing resistors (R151 to R162) and the IC internal resistance. To reduce the output current when the IC is not operating and oscillation is stopped, implement design using an auxiliary winding type, as described in Section 3.3.

Figure 11 shows the internal circuit diagram and voltage waveforms for the Svin and Svout pins.

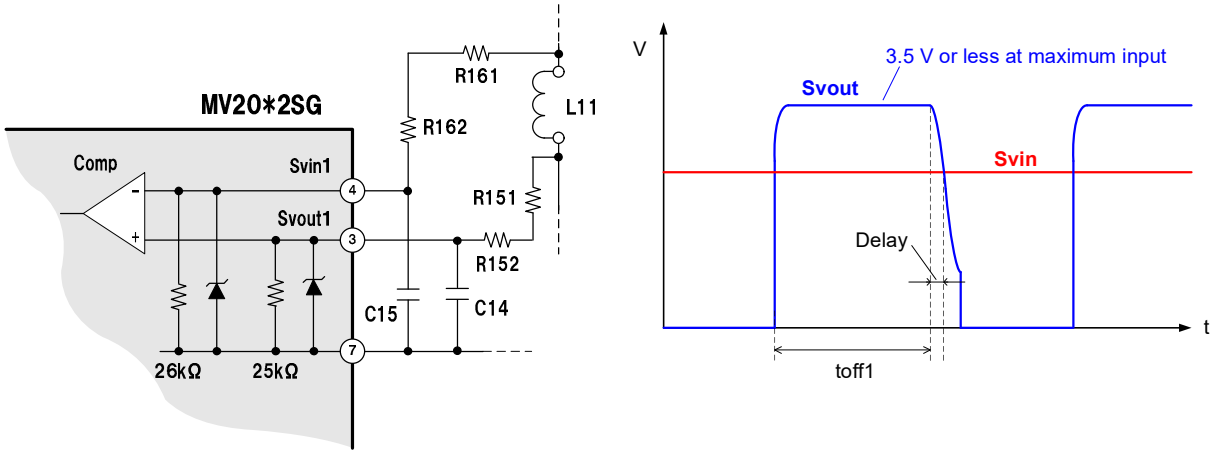


Figure 11 Internal circuit diagram and zero current detection operation waveforms

Select R151 and R152 (R251 and R252) using the following formula so that the Svout pin voltage is around 3 V for the maximum input voltage:

$$R151 + R152 = \frac{25k \times (Vi\_max + V_F)}{3} - 25k$$

$$R161 + R162 = R151 + R152$$

The internal pull-down resistors for the Svin and Svout pins are set to 26 kΩ and 25 kΩ, respectively, creating an approximate 4 % difference in resistance. Making R161 + R162 and R151 + R152 equal ensures that the Svin voltage is always greater than the Svout voltage during LED short-circuits, preventing erroneous turn-ons due to noise.

When selecting the external resistors for the Svin and Svout pins, use high-accuracy resistors not exceeding ±1 %.

Note that zero current detection may not be possible for specifications where the output voltage Vo does not exceed 10 % of the maximum input voltage Vi. In such cases, implement design using an auxiliary winding type, as described in Section 3.3.

3.2.7 CS pin filter selection (R12 + C12, R22 + C22)

R12 (R22) and C12 (C22) are filters used to shield the CS pin from noise. Adjusting R12 to a range between 0 Ω and several kΩ and C12 between 10 pF and 100 pF will reduce false off-timing detections caused by turn-on noise in the off-time modulation region. When adjusting the filter constants, check for false detections on the actual apparatus using as many different REF pin voltage V_{REF} settings as possible within the specified REF voltage range. (For details, refer to “5.1.2 [B] Off-time modulation region” on pages 26 to 27.)

Setting the filter constants too large will increase detection delays, causing the output current fluctuations to increase due to the output current and input voltage settings. Reselect the current detection resistors and inductors as necessary.

3.2.8 Vcc pin smoothing capacitor selection (C2)

C2 is a capacitor used to stabilize the power supply voltage for the Vcc pin. Check the Vcc pin voltage waveform and select a capacitor with a minimum capacitance of 0.1 uF. Check on the actual apparatus, as selecting an exceptionally high capacitance will increase the startup time.

3.2.9 REF pin capacitor selection (C13, C23)

C13 (C23) is a capacitor used to prevent unintended operations due to noise. Use a capacitor with a capacitance of approximately 1,000 pF. For details of dimming methods, refer to “5. Dimming Characteristics” on page 24.

3.2.10 Svin pin capacitor selection (C15, C25)

C15 (C25) is a capacitor used to prevent unintended operations due to noise. Use a capacitor with a capacitance of approximately 1,000 pF.

3.2.11 Resonant capacitor selection (Cr1, Cr2)

Adding a resonant capacitor Cr1 (Cr2) allows the resonance period to be adjusted and helps reduce turn-off noise. However, note that it may also sometimes increase turn-on noise. If Cr is large, dimming characteristics and efficiency will be degraded, therefore in general we recommend against using this capacitor. If the capacitor becomes necessary, adjust on the actual apparatus to minimize capacitance.

3.2.12 Input capacitor (C101) and output capacitor (C111, C211) selection

Select the input and output capacitors taking into account factors such as the allowable ripple current, life, and output holding time. The capacitor ripple current is calculated using the following formulas:

Input capacitor ripple current

$$Iripin = Ip1 \times \sqrt{D1 \times \left(\frac{1}{3} - \frac{D1}{4}\right)} + Ip2 \times \sqrt{D2 \times \left(\frac{1}{3} - \frac{D2}{4}\right)}$$

Output capacitor ripple current

$$Iripout = \frac{Io}{\sqrt{3}}$$

Where Ip1 and Ip2 represent the peak currents for L11 and L21, and D1 and D2 represent the switching duty for channel 1 and channel 2.

D is given by the following formula based on the relationship between input and output voltages:

$$D1 = \frac{Vo1}{Vi} \qquad D2 = \frac{Vo2}{Vi}$$

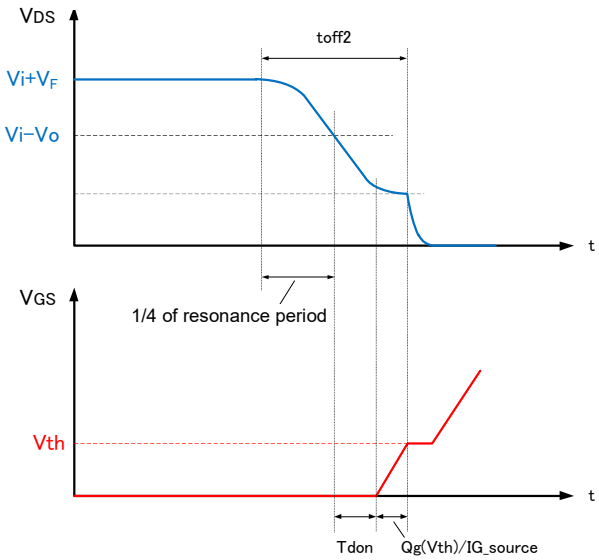
With the input capacitor, ripple from the input circuit side, such as full-wave rectification or PFC, will be overlaid. This must be taken into account when selecting the capacitor.

3.2.13 Svout pin capacitor selection (C14, C24)

C14 (C24) is a capacitor used to adjust the delay shown in Figure 11 and to adjust the on-timing. The resonance period varies depending on components such as inductors and MOSFETs. Adjusting the delay so that toff2 in Figure 12 is half the resonance period causes the MOSFET to turn on at the trough resonance voltage, minimizing switching losses and noise. A larger C14 increases the delay, so the optimal range is typically between around 10 pF and 100 pF. We recommend a C14 with a capacitance of at least 10 pF to prevent noise-induced malfunctions.

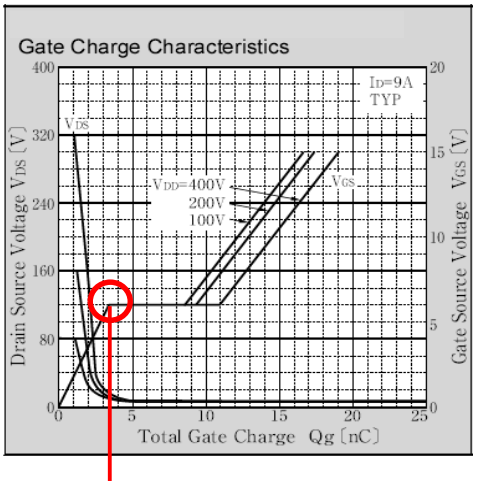
Additional explanation of resonance period in quasi-resonant operation

Enlarged view of Vds in Figure 6



Tdon: Response delay

Typical gate charge characteristics



Qg(Vth): Accumulated charge until voltage reaches gate threshold

Figure 12 Delay time adjustment

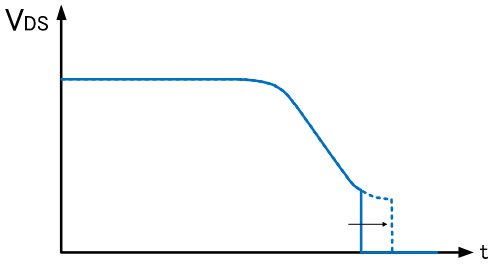
Ideally, the MOSFET should be turned on at a resonance trough, as shown in Figure 12, the corresponding conditions of which are expressed by the following formula:

$$\frac{1}{4}\times 2\pi\sqrt{L\times(Cr+Coss+Cj)} = Td_{on} + \frac{Qg(Vth)}{Ig}$$

Coss: MOSFET output capacitance Cr: Capacitor capacitance across D and S
Cj: Regenerative diode junction capacitance

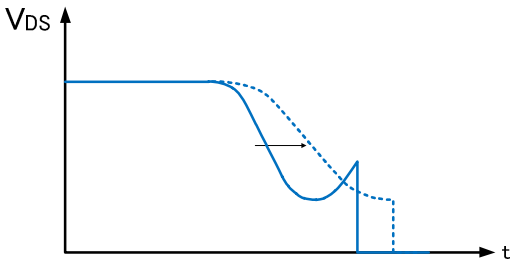
Since Vb = Vi - 2Vo - V_F, switching losses are minimized. While these conditions may not be completely satisfied in practice, MOSFETs do not need to be turned on precisely at a trough. If the on-timing is too far from the trough, it can be adjusted as follows:

(1) When left side is large



⇒ Delay on-timing.
・Increase C14 (C24) or R13 (R23).

(2) When right side is large



⇒ Increase resonance period.
・Increase Cr1 (C22).

3.3 Types using auxiliary windings

3.3.1 Circuit configuration for types using auxiliary windings

As shown in Figure 13, using auxiliary windings protects the MV2002SG and MV2052SG against output overvoltages—for example, when LEDs are open-circuit. It also ensures reliable operation even with specifications according to which output voltage Vo does not exceed 10 % of the maximum input voltage Vi. (Refer to “3.2.6 Svin and Svout pin resistance selection” on page 16.)

When selecting components, select the appropriate auxiliary windings and rectifier diodes for the auxiliary windings.

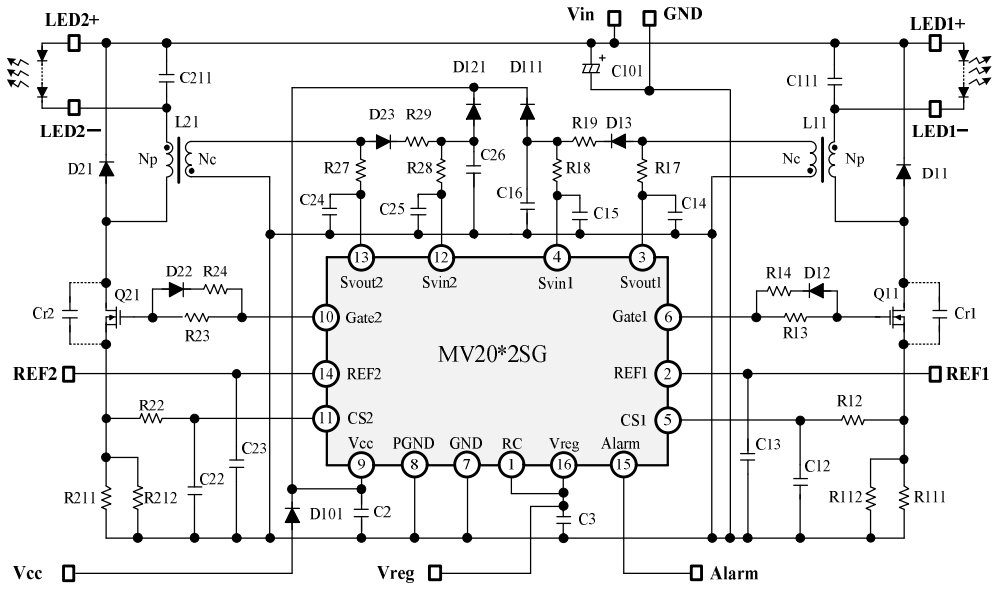


Figure 13 Circuit configuration for types using auxiliary windings

3.3.2 Auxiliary winding (Nc) selection

If Vc represents the auxiliary winding voltage rectified and applied to the Vcc pin, we can obtain Vc using the formula below. Select the turn ratio to ensure that voltage Vc is within the range of 10 V to 16 V, accounting for Vo fluctuations due to dimming and LED VF variations.

$$\frac{Nc}{Np} \cong \frac{Vc}{Vo}$$

Np: Number of inductance windings [T]
Nc: Number of auxiliary windings [T]

Depending on the turn ratio and winding coupling conditions, a surge voltage may be generated in the auxiliary windings that exceeds the Vc voltage setting. Check on the actual apparatus to ensure the Vc voltage is between 10 V and 16 V.

3.3.3 Auxiliary winding rectifier diode (D13, D23) selection

The reverse voltage Vr represented by the following formula is applied to D13 (D23). Note the withstand voltage when selecting this component.

$$Vr = Vi \times \frac{Nc}{Np}$$

When the input voltage is at maximum, the reverse voltage across D13 will also be at maximum. Note that a fast recovery diode (FRD) should be used for D13.
(Refer to Table 4 Recommended rectifier diodes.)

Table 4 Recommended rectifier diodes (as of January 2016)

Product name	Withstand voltage (V)	Io (A)	V_F (V)	Cj (pF)	trr (ns)	Manufacturer	Package
M1FL20U	200	1.1	0.98	-	35	Shindengen	M1F
M1FL40U	400	1.5	1.2	11	25	Shindengen	M1F
D1FK60	600	0.8	1.3	11	75	Shindengen	1F

Inserting a resistor R19 (R29) in series with D13 can curb the increase in voltage Vc due to the auxiliary winding surge voltage.
R17 (R27) should be 1 MΩ, and R18 (R28) should be 220 kΩ.

The Svin and Svout pin waveforms will be as shown in Figure 14 when using auxiliary windings.

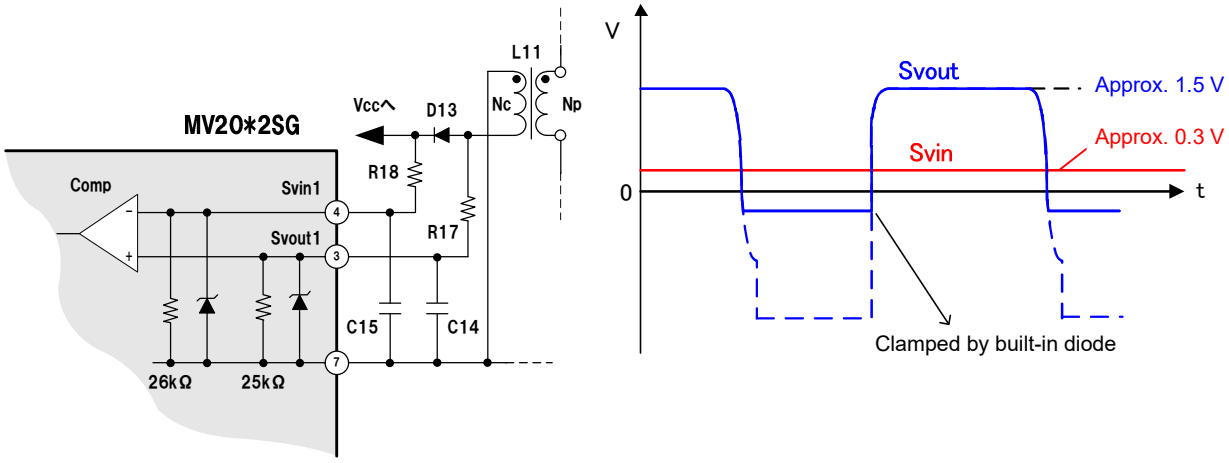


Figure 14 Svin and Svout pin waveforms for types using auxiliary windings

3.3.4 LED open protection using auxiliary windings

Inductor auxiliary windings configured as shown in Figure 13 can be used to protect against output overvoltage—for example, when LEDs are open-circuit. The Vcc pin includes a latch stop function for when an overvoltage is detected, disabling operation when the Vcc pin voltage reaches 20.7 V (typical). If the auxiliary windings are wound with the polarity shown in Figure 13, the auxiliary winding voltage will be proportional to the output voltage. This makes it possible to indirectly detect an overvoltage caused by an LED open-circuit and to use Vcc overvoltage protection to latch-stop operation.

The output voltage Vovp at the time of latch stop can be calculated using the following formula:

$$Vovp = \frac{20.7}{Vc} \times Vo$$

Note that with specifications according to which the difference between the input voltage Vi and the output voltage Vo is small, the Vcc voltage may not reach 20.7 V. The auxiliary windings may not provide LED open-circuit protection in these cases.

4. Pattern Design Precautions

4.1 Precautions

Figure 15 shows the same circuit as in Figure 5, rearranged to account for pattern design. The following four points must be carefully considered during pattern design. In particular, as described in item 1, each signal line should be wired as far as possible from the main path or gate lines of other channels to prevent turn-off noise from affecting the other channel.

1. The area enclosed in the dotted lines is the control circuit. The control circuit should be designed to minimize the effects of noise and magnetic flux from the main circuit. Ideally, the control circuit should have a single ground terminal connected to a stable part of the main circuit, such as a negative pin of the input capacitor. Pay particular attention to the wiring for signals input to the REF, Svin, Svout, and CS pins: keep the tracks as far away as possible from high-voltage circuits. Avoid routing them close to the main path or gate lines of other channels.
2. The shaded area indicates the main circuit through which the switching current flows. Keep the wiring as short as possible to minimize the area occupied. Route the current paths for channels 1 and 2 separately, as shown in Figure 15.
3. Magnetic flux is generated near the inductor. Use a closed magnetic path inductor with low magnetic flux leakage and avoid running signal lines directly beneath the inductor.
4. Route the tracks for the Svin and Svout pins for the same channel as near to parallel as possible.

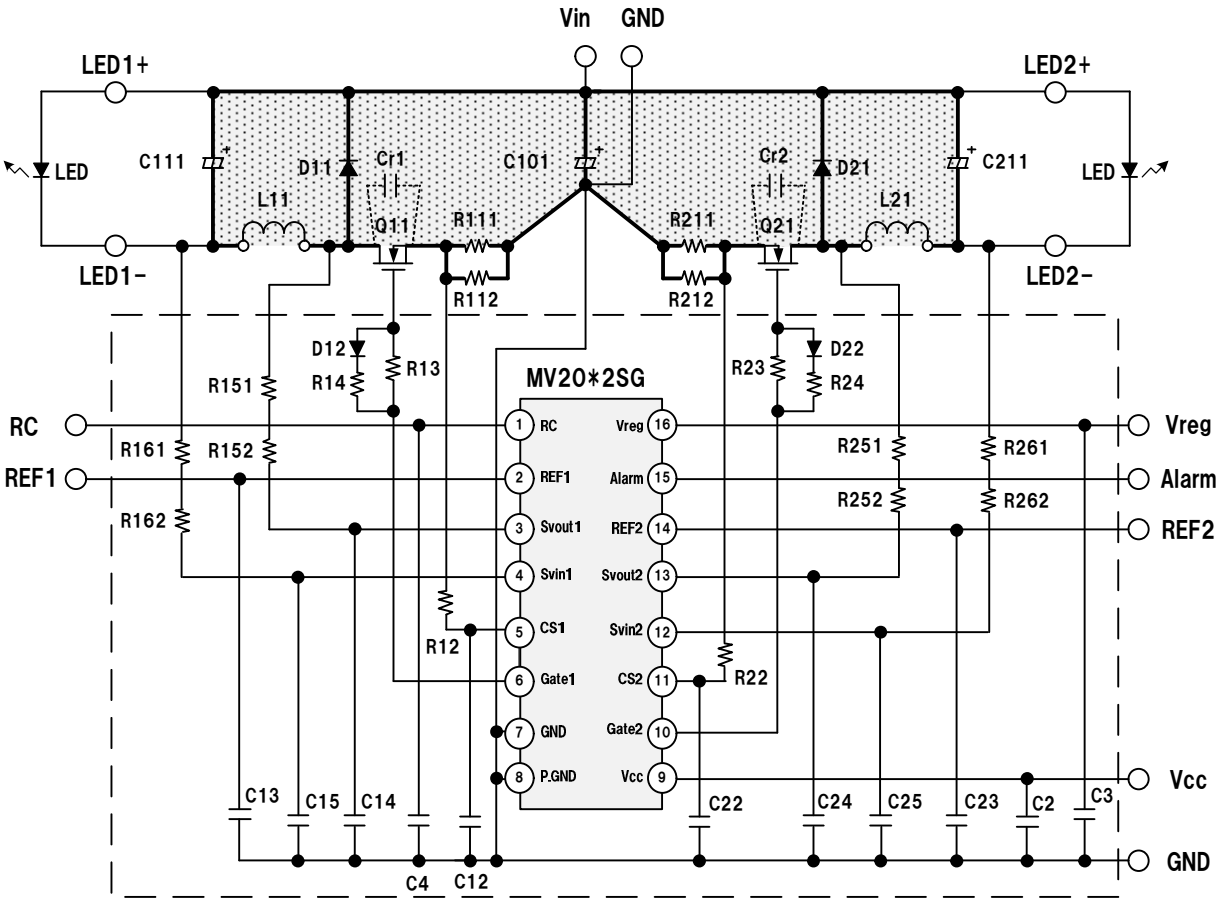


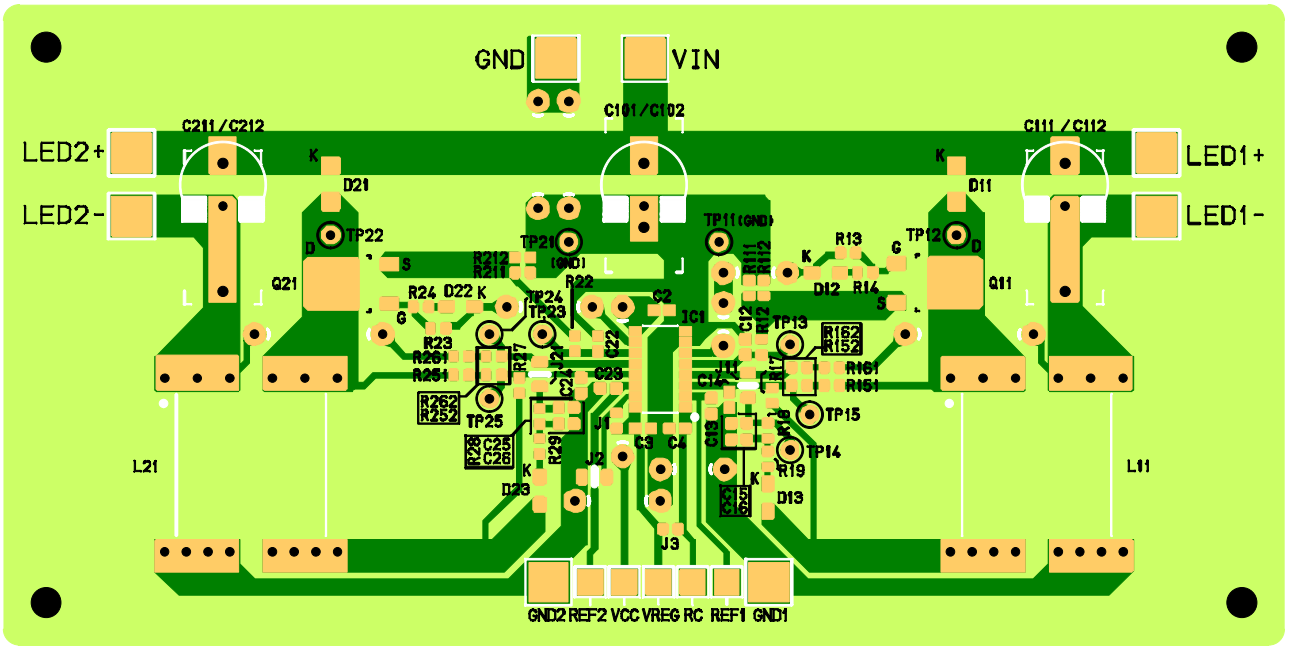
Figure 15 Circuit diagram accounting for pattern design

4.2 PCB pattern example

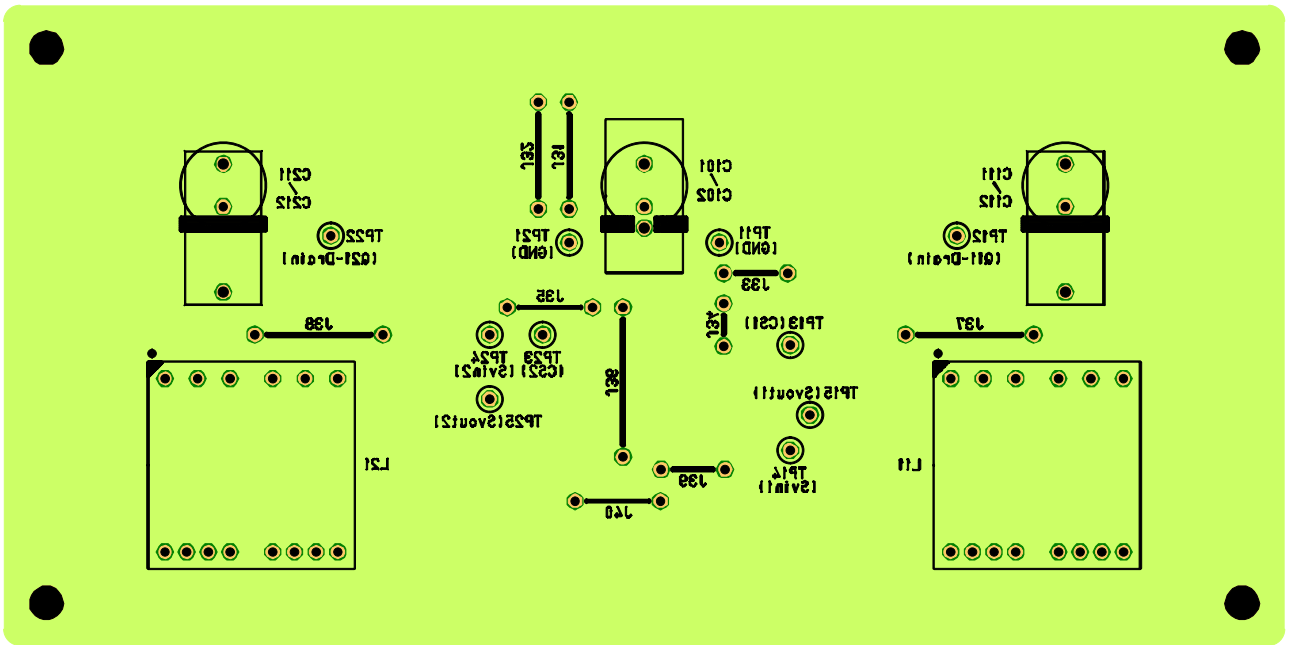
Shown below is a reference pattern using a Shindengen sample board. The sample board pattern does not include an input fuse or input line filter. These should be added for actual use.

The pattern shown below is provided as an example. It does not guarantee actual operation. Be sure to verify operation on the actual apparatus.

<Top>



<Underside>



[PCB size: 75 mm (H) × 150 mm (W)]

5. Dimming Characteristics

Figure 16 shows typical dimming characteristics for the MV2002SG and MV2052SG.

The reference voltage at the CS pin is varied internally within the IC according to the REF pin voltage V_{REF}. V_{REF} can therefore be adjusted to adjust the peak current, enabling linear dimming. Reducing the off-time automatically switches from current critical operation to current discontinuous operation, enabling linear dimming down to very low output currents. PWM dimming is also possible by applying a PWM signal of 1 kHz or less to the REF pin and controlling the PWM signal duty.

Mode switching between the [A] frequency modulation region and [B] off-time modulation region shown in Figure 16 is performed automatically by comparing Toff (CRM) and Toff (DCM) inside the IC. Toff (CRM) is the off-time in current critical mode (sum of toff1 calculated using the formula in Figure 6 on page 11 and the resonance period toff2), and Toff (DCM) is the forced off-time determined inside the IC based on V_{REF}. When Toff (CRM) > Toff (DCM), the operation mode switches to the [A] frequency modulation region. When Toff (CRM) < Toff (DCM), the operation mode switches to the [B] off-time modulation region. The REF pin voltage for mode switching varies depending on parameters such as the input/output conditions and choke coil inductance. The forced off-time Toff (DCM) should be calculated using the following approximation formula as a guide:

$$Toff\ (DCM) \cong \frac{195.5}{206 \times V_{REF}{}^2 + 62 \times V_{REF} - 45} + 0.3 \quad [\mu s] \quad (0.4V < V_{REF} < 0.75V)$$

The lower graph in Figure 16 is an example of REF pin voltage plotted against off-time. The red curve represents Toff (CRM), while the green curve represents Toff (DCM). Note that if V_{REF} is equal to or less than (Vth_REF_st - Vth_REF_hys), operation will switch to the [C] oscillation stop region.

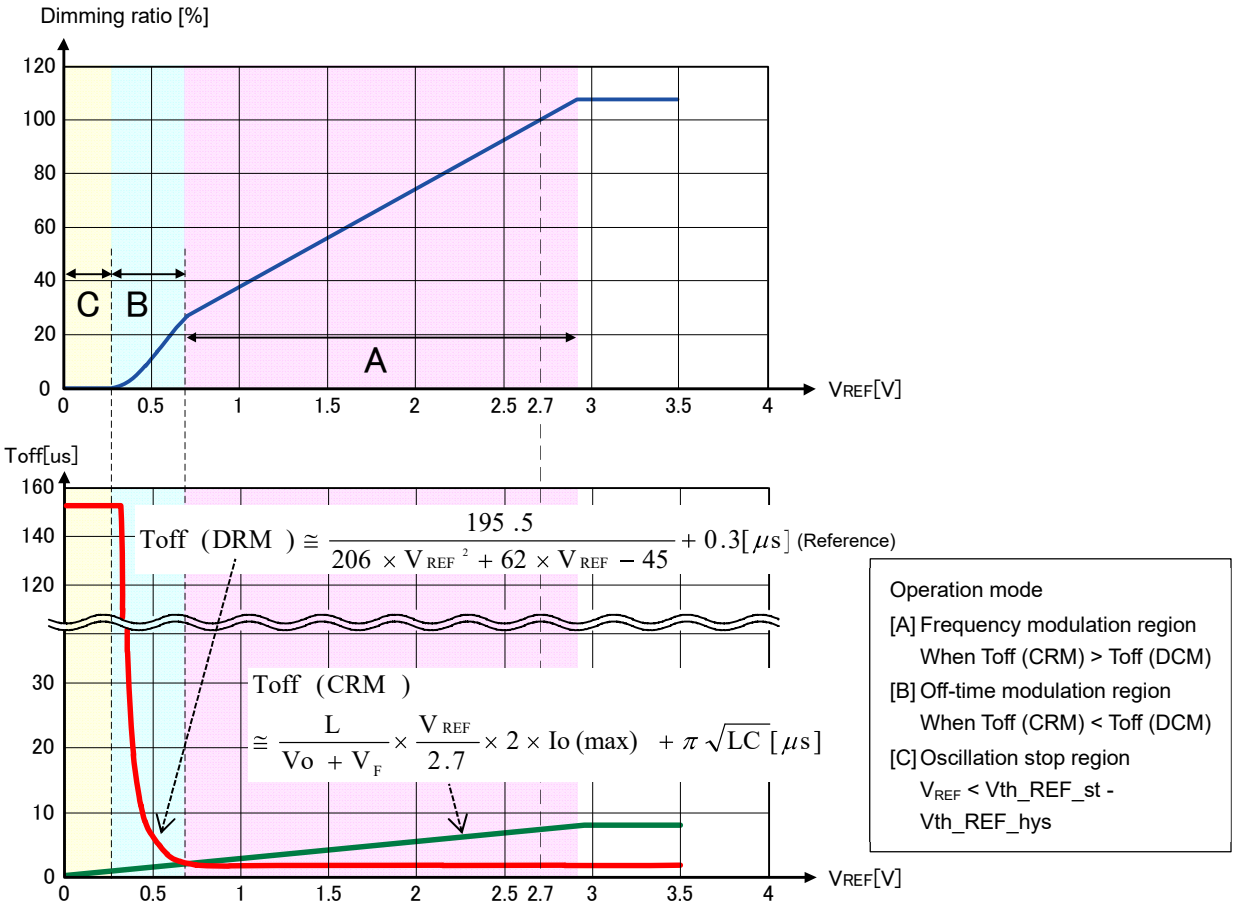


Figure 16 Relationship between REF pin voltage V_{REF} and dimming ratio and off-time Toff

5.1 Mode operations

5.1.1 [A] Frequency modulation region

In the frequency modulation region, the operation waveforms will be current critical operation waveforms, as shown in Figure 18. Figure 17 shows the internal circuit of the CS pin. The voltage corresponding to one-fifth of V_{REF} is compared against the current detection threshold voltage Vth_CS (0.585 V), and the lower of the two is used as the CS pin reference voltage. In a circuit in which Vth_CS and V_{REF} are reduced to 1/5, the latter will have smaller fluctuations. To improve relative current accuracy for channels 1 and 2, implement design so that the rated current is achieved for a V_{REF} not exceeding Vth_CS. (Ideally, set to achieve the rated current when V_{REF} is 2.7 V.) For reliable use of Vth_CS as the reference voltage, set V_{REF} to at least 3.3 V, accounting for the voltage variations between Vth_CS and V_{REF} × 1/5.

If the resonance period toff2 is sufficiently short compared to ton and toff1, IL can be treated as a triangle wave. This means Io = 1/2 × Ip; the output current Io will be proportional to V_{REF}. However, since the oscillation frequency increases as V_{REF} decreases, the ratios of toff2 and the detection delay for each cycle will increase, somewhat changing the proportional relationship between Io and V_{REF}.

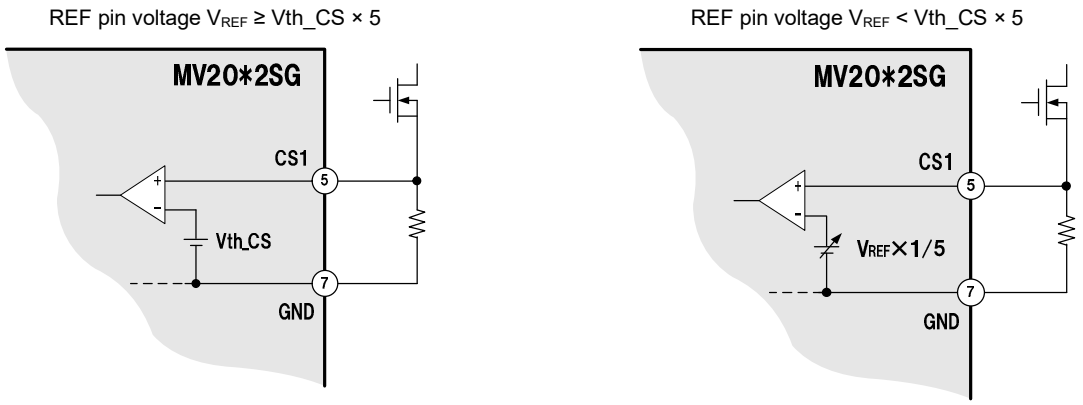


Figure 17 CS pin internal circuit diagram

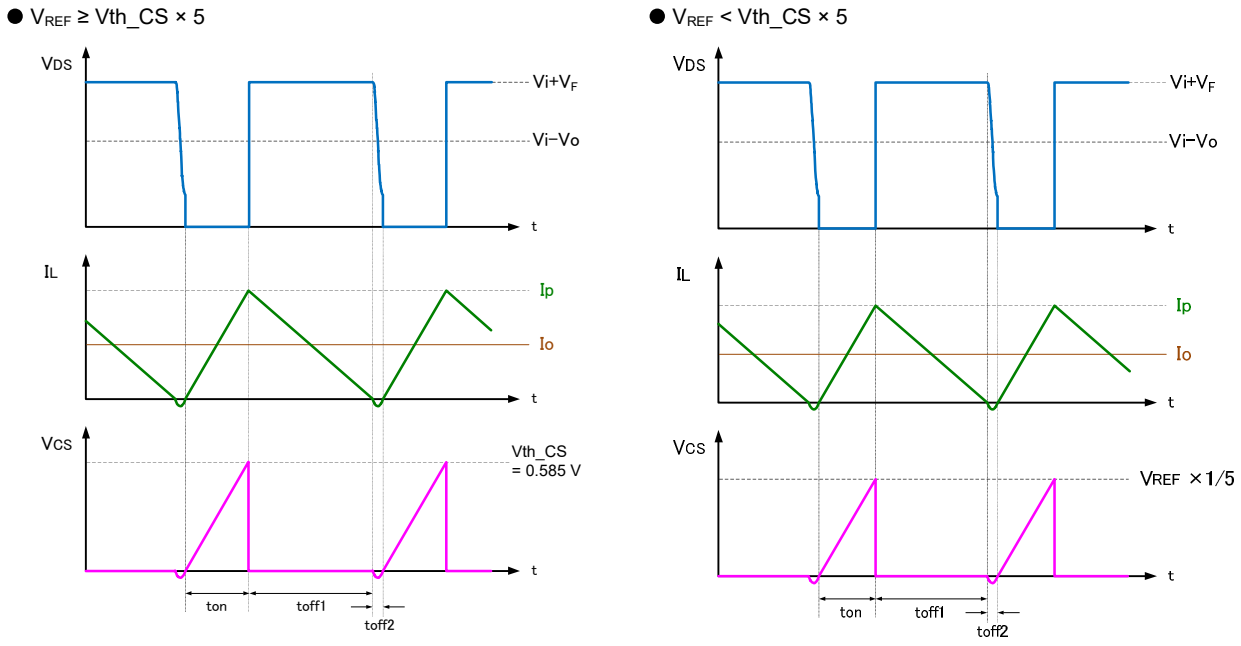


Figure 18 Operation waveforms in [A] frequency modulation region

5.1.2 [B] Off-time modulation region

In the off-time modulation region, the operation waveforms will be current discontinuous operation waveforms, as shown in Figure 19. The output current can be controlled to extremely low levels by increasing the forced off-time toff (DCM) as V_{REF} falls. Note that the forced off-time includes toff1, the period during which a current flows through D11 (D21). As shown by the formula in Figure 6, toff1 is dependent on Vo; if Vo changes, Io in the [B] region will also change.

The reference voltage for the CS pin is also one-fifth of V_{REF} in the [B] region. Since V_{REF} is lower than in the [A] region, the reference voltage will also be lower than in the [A] region. This means the circuit will be more susceptible to noise at the CS pin in the [B] region, and the MOSFET will be more likely to turn off at a timing that differs from the timing of peak current detection. The turn-on timing does not coincide with a trough in the resonant voltage, so the V_{DS} voltage at turn-on is higher than Vb, increasing turn-on noise. A leading edge blanking (LEB) period is provided in which noise is rejected after turn-on to prevent the MOSFET from being turned off. (Figure 20 (b)) However, if turn-on noise or noise from an external circuit exceeds the reference voltage for the CS pin even after the LEB period, the MOSFET will be turned off due to false detection of this noise. (Figure 21 (b)) As a result, Io will drop below the normal level, possibly causing LED flicker, depending on the timing of the noise.

If Coss of the MOSFET, Cr of the resonant capacitor, or Cj of the regenerative diode is large, the turn-on noise will also be large. If turn-on noise causes false detection, adjust the CS filter (page 17), adjust the gate resistance (page 16), or reselect the components above.

One way to easily check whether false detection has occurred is to use many different V_{REF} settings and check the gate waveform for an obviously short ton that is not peak current detection. Operations may change if the V_{cs} and V_{DS} voltages are measured here. We therefore recommend measuring just the gate pin waveform when checking.

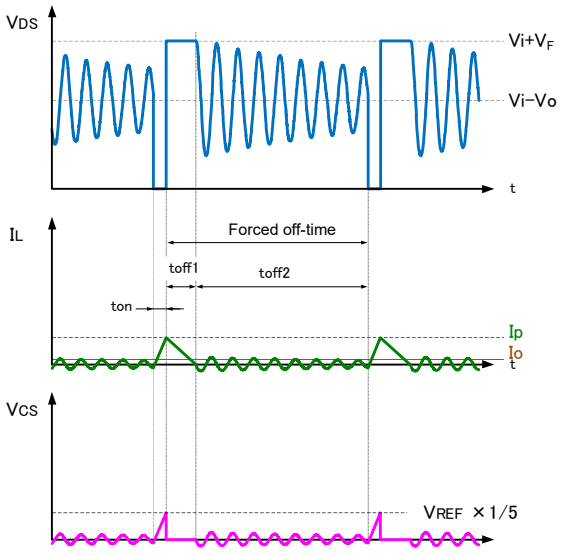


Figure 19 Operation waveform in the [B] off-time modulation region

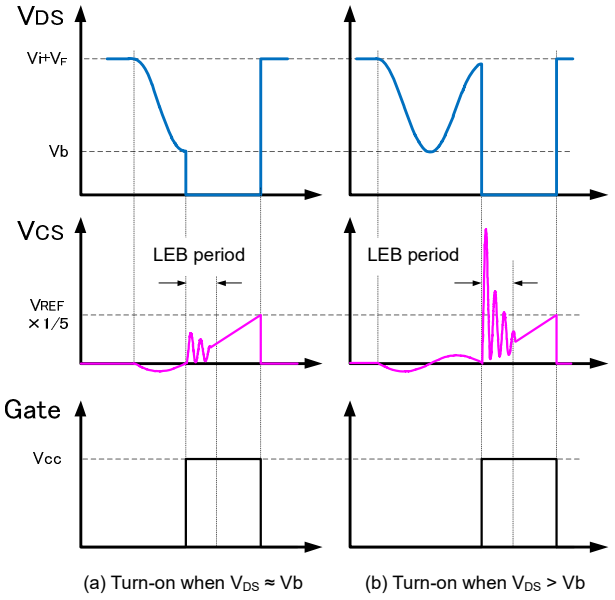


Figure 20 Example of turn-on noise caused by V_{DS}

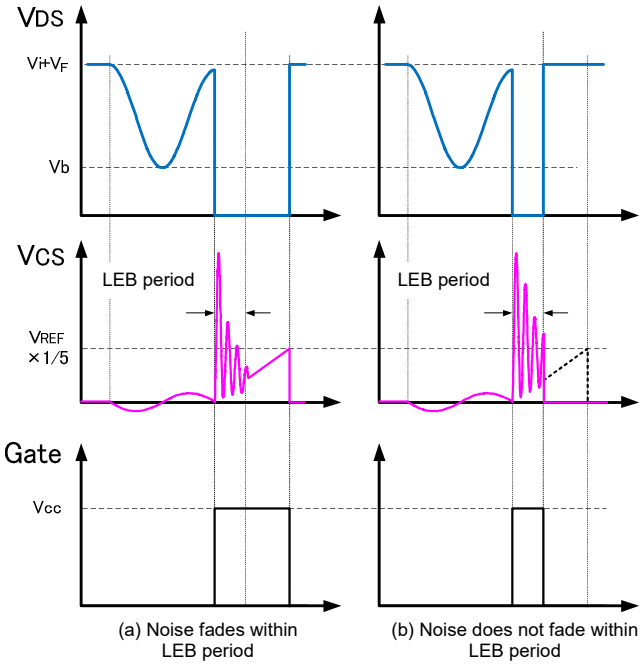


Figure 21 Example of false detection due to turn-on noise

The resonant current flowing during the toff2 period also flows through the current detection resistor Rcs. Thus, Vcs oscillates around 0 V during the toff2 period. As shown in Figure 22, even with the same V_{REF}, Io accuracy and the smoothness of dimming characteristics may be degraded if the on-time changes significantly, depending on whether Vcs at turn-on exceeds 0 V (see small V_{REF} ripple in Figure 23).

The amplitude of Vcs oscillation during the toff2 period can be minimized by reducing the Coss of the MOSFET and the Cr of the resonant capacitor. The V_{REF} ripple voltage can also be increased to average out any on-time changes and to reduce Vcs-dependent changes in Io at turn-on. (See large V_{REF} ripple in Figure 23.)

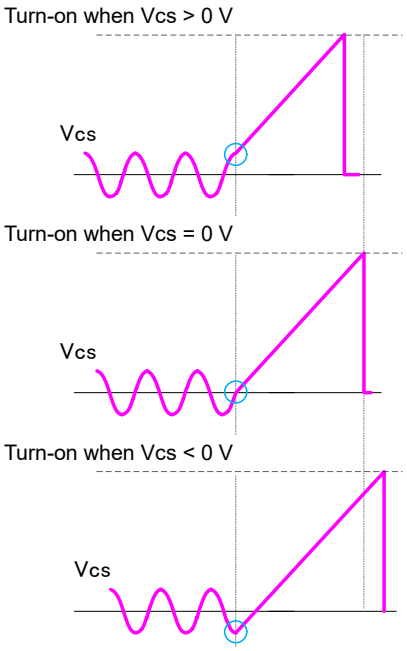


Figure 22 Changes in on-time due to turn-on timing in the [B] region

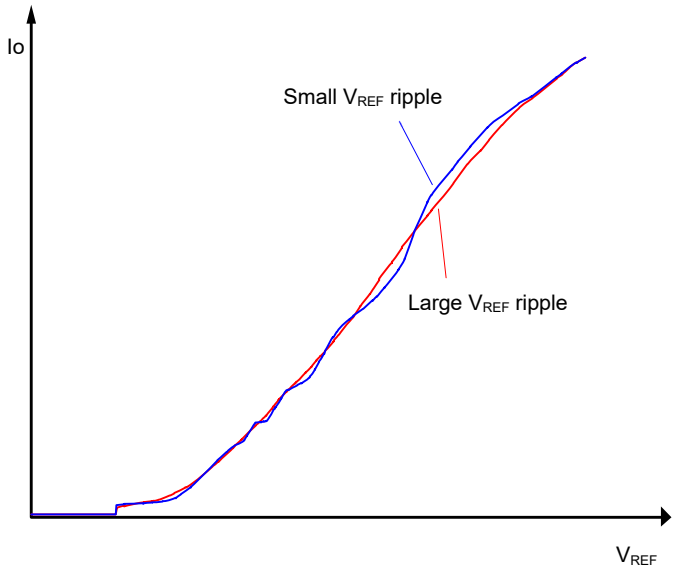


Figure 23 Example illustrating degraded smoothness of dimming characteristics

5.1.3 [C] Oscillation stop region

The MV2002SG and MV2052SG allow gate oscillation to be stopped by holding V_{REF} at or below (Vth_REF_sp - Vth_REF_hys). To turn the MOSFET completely off, Io can be brought closer to zero than in the [B] region.

In the basic circuit configuration shown in Figure 5, a leakage current flows constantly via the internal resistors of the Svin and Svout pins. The leakage current is also present in the [A] and [B] regions. However, in the [C] region, in which the MOSFET is completely off, Io is simply the leakage current. The value of this leakage current is determined by the input/output voltage difference and the values of resistors R151, R152, R161, and R162 (R251, R252, R261, and R262). To eliminate the leakage current, configure a circuit of the type using auxiliary windings.

Note that the standard values for Vth_REF_st and Vth_REF_hys vary. Set V_{REF} to no more than 0.12 V for reliable use of the [C] region.

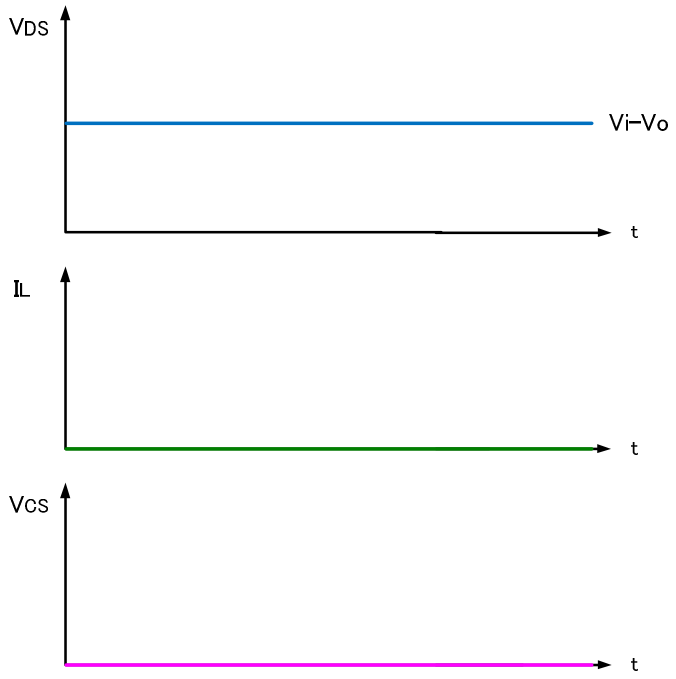


Figure 24 Operation waveform in the [C] oscillation stop region

5.2 PWM dimming

5.2.1 PWM dimming in 100 % and oscillation stop regions

PWM dimming can be performed by applying a PWM signal to the REF pin corresponding to V_{REF} (2.7 V here) for 100 % dimming as the high level and corresponding to V_{REF} for the oscillation stop region as the low level. PWM signal frequency f and on-duty cycle Don, respectively, should be 1 kHz or less and 1 % or more.

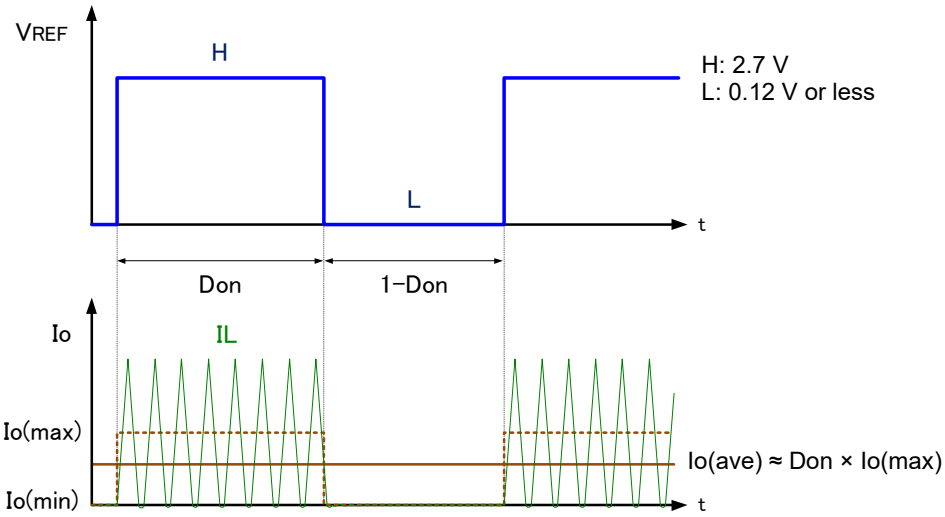


Figure 25 Example of PWM dimming operation

As shown in Figure 25, when a PWM signal with an on-duty cycle of Don is applied to the REF pin, Io becomes the average current Io(ave) = Don × Io(max) + (1 - Don) × Io(min). In practice, Io(min) is negligible, and the equation can be rewritten as Io(ave) ≈ Don × Io(max).

With PWM dimming, if the initial turn-on timing in the H-signal period is irregular, the effective Don will become irregular as well, making Io unstable. This effect is especially significant if Don is small. The initial turn-on timing in the H-signal period of every cycle is therefore aligned by detecting a change in V_{REF} from the L signal to H signal and forcibly outputting an on-trigger. This function helps stabilize Io(ave), even when Don is small.

5.2.2 Combination of linear dimming and PWM dimming

One way to achieve good output current accuracy throughout the range from 100 % rated current to very small currents is to combine linear dimming and PWM dimming, as shown in Figure 26.

Assume V_{REF}_any represents any given REF voltage in the [A] region and Io' represents Io at that voltage. For Io' or more, linear dimming is used, and for Io' or less, PWM dimming is used. Assume the PWM dimming signal for high level is V_{REF}_any, and V_{REF} in the oscillation stop region for low level. Combining the dimming methods in this way allows dimming down to smaller currents than with PWM dimming alone, and achieves control with better output current accuracy than with linear dimming alone.

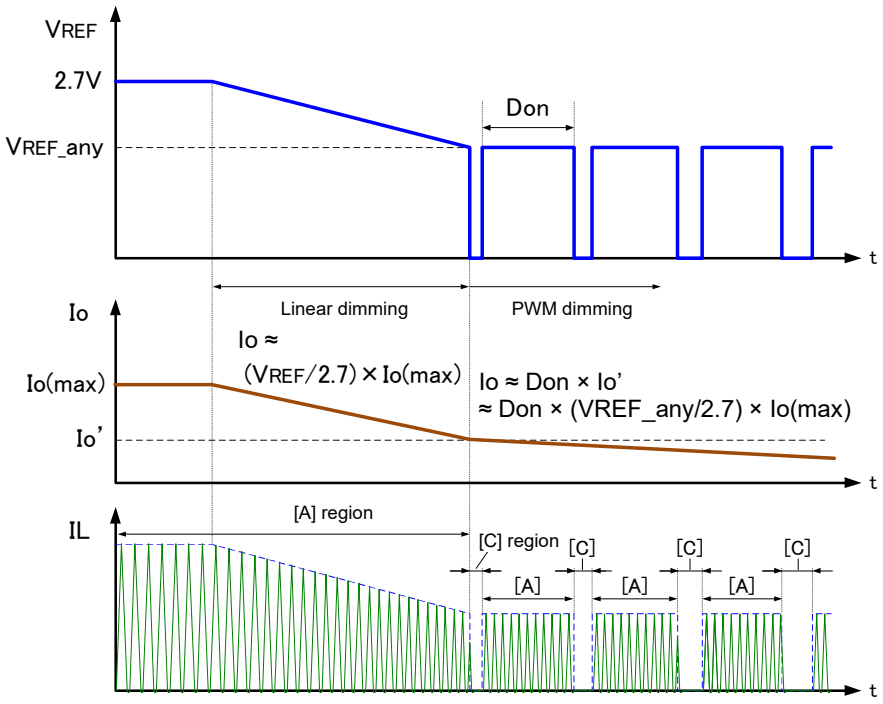


Figure 26 Dimming using combination of linear dimming and PWM dimming

5.3 Dimming circuit

As the REF terminal of the MV2002SG and MV2052SG is internally pulled down inside the IC, an external voltage must be applied to start oscillation. An example circuit for smoothing the PWM signal is provided below as a reference for external dimming circuits.

5.3.1 Example of dimming circuit for smoothing PWM signal

Figure 27 shows an example of a dimming circuit that smoothes a PWM dimming signal and applies it to the REF pin. Assuming that V_{REF}_L represents V_{REF} when the transistor Q101 is turned on and that V_{REF}_H represents V_{REF} when the transistor is turned off in Figure 27, the approximate values of these voltages can be obtained using the formulas given below.

$$V_{REF}\_H = V_{DD} \times \frac{R102}{(R101 + R102)}$$

$$V_{REF}\_L = I\_ref \times (R103 + R104)$$

If V_{REF}_H is 3.3 V or higher, the dimming range is reduced, so, based on the formula above, set the value for resistors R101 + R102 to achieve a voltage of approximately 2.7 V. Apply a stable voltage: dimming accuracy will be affected if the V_{DD} voltage varies significantly.

The components R103, R104, C101, and C102 smooth DC voltages V_{REF}_H and V_{REF}_L, and the V_{REF} value obtained using the formula given below is applied to the REF pin. Adjust the capacitance of C101 and C102 to approximately 1 uF while checking dimming characteristics.

$$V_{REF} = (1 - Don) \times V_{REF}\_H + Don \times V_{REF}\_L$$

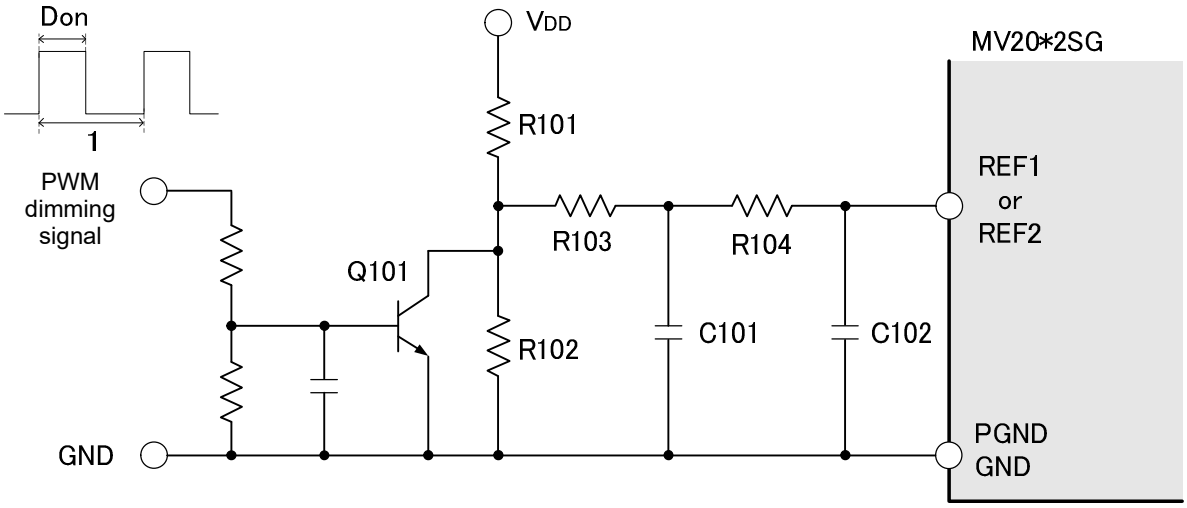


Figure 27 Typical PWM dimming signal smoothing circuit

6. Operations in Abnormal Situations

While the MV2002SG and MV2052SG incorporate various protection functions, there are some abnormal modes in which the IC functions alone cannot provide adequate protection.
The main operations occurring for abnormal situations are described below as a guide. For details of the alarm signal output in abnormal situations, refer to “2.4 Alarm signal output function” on page 10.

Note that testing for situations such as open-circuit and short-circuit should ultimately be performed on the actual apparatus to check operations in abnormal situations.

6.1 LED open-circuit

A latch stop function is provided to protect against LED open-circuits using the auxiliary winding voltage and Vcc_OVP function. For details, refer to “3.3.4 LED open protection using auxiliary windings” on page 21.

① With auxiliary windings:
⇒ The output voltage is detected indirectly using the auxiliary winding voltage, and latch stop is performed by the Vcc_OVP function.

② Without auxiliary windings:
⇒ The IC operates with the maximum on-time, Ton_max, and Vo is approximately equal to Vi. An alarm signal is output if Ton_max persists for 128 cycles.
The withstand voltage of the output capacitor should be the same as that of the input capacitor.

6.2 LED short-circuit

If Vo becomes 0 V, the operation automatically switches from zero current detection to restart operation. This makes it possible to forcibly limit the current in the event of an LED short-circuit. After the short-circuit has been resolved and the output voltage rises, the IC is automatically reset and begins to operate with zero current detection.

Note that if the formula below is satisfied, the IC operates in current continuous mode, and any short-circuit current flowing through the MOSFET or regenerative diode is likely to increase. Check on the actual apparatus to ensure that no problems arise even in such cases.

$$Vi > \frac{Trestart}{Ton\_min} \times V_F$$

V_F here is the forward voltage at the regenerative diode D1.

Figure 28 shows ideal waveforms for the Svout and Svin pins in the event of an LED short-circuit. Make sure the Svin voltage always exceeds the Svout voltage in the event of an LED short-circuit. To prevent false turn-ons due to noise, the internal pull-down resistors for the Svin and Svout pins have been set to differ by about 4 % to 26 kΩ and 25 kΩ, respectively. To protect against noise, insert capacitors close to the Svin and Svout pins. (Refer to Sections 3.2.10 and 3.2.13.)

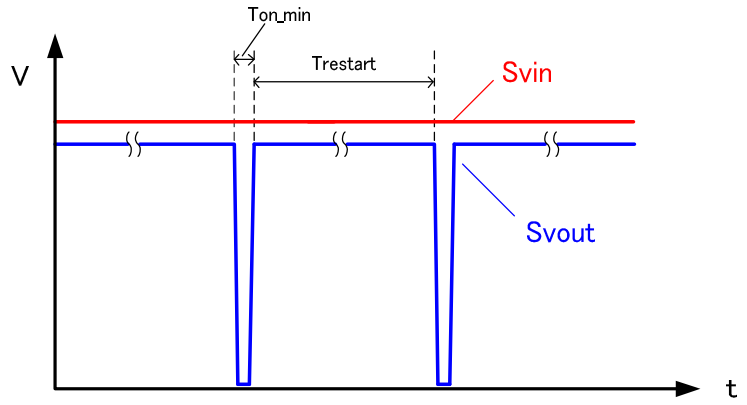


Figure 28 Svin and Svout pin waveforms in the event of an LED short-circuit

6.3 Overheating

The MV2002SG and MV2052SG incorporate an internal overheat protection function. If the junction temperature (Tj) of the IC reaches the overheat protection stop temperature (approximately 150 ºC), overheat protection is triggered, and oscillation stops for both channels. The IC resets automatically once Tj falls to approximately 50 ºC below the stop temperature.

Overheat protection will not function if components other than the IC overheat. Install separate protection circuits as necessary.

6.4 CS pin open-circuit

If a CS pin open-circuit occurs, Vcs rises due to the internal pull-up current, and remains above the CS pin reference voltage. In the event of a CS open-circuit in which Vcs rises, only the affected channel will latch-stop. An alarm signal is output when operation stops. To restore operation, clear the CS open-circuit, and reset using either Vcc or RC.

6.5 Short-circuit between CS and GND pins

Peak current detection is unavailable at the CS pin, and the IC operates using the maximum on-time Ton_max. If Ton_max operation reaches 128 consecutive cycles, protection will trigger only for the channel with the CS-GND short-circuit, causing the IC to operate using Ton_max and Toff_max. Operation is automatically restored once the short-circuit has been cleared, making zero current detection possible again.

6.6 Current detection resistor open-circuit

The MOSFET source floats, making MOSFET operation unstable for the channel for which the current detection resistor is open-circuit. If the MOSFET switches off, Io will become nearly zero. However, if the MOSFET is on, a CS pin overvoltage will occur, potentially damaging the IC. Install separate protection circuits as necessary.

6.7 Current detection resistor short-circuit

Since Vcs becomes close to the GND level, the IC operates using the maximum on-time Ton_max. If Ton_max operation reaches 128 consecutive cycles, protection is triggered only for the channel with the current detection resistance short-circuit, causing the IC to operate using Ton_max and Toff_max. Operation is automatically restored once the short-circuit has been cleared, making zero current detection possible again.

7. Standard Circuit Example

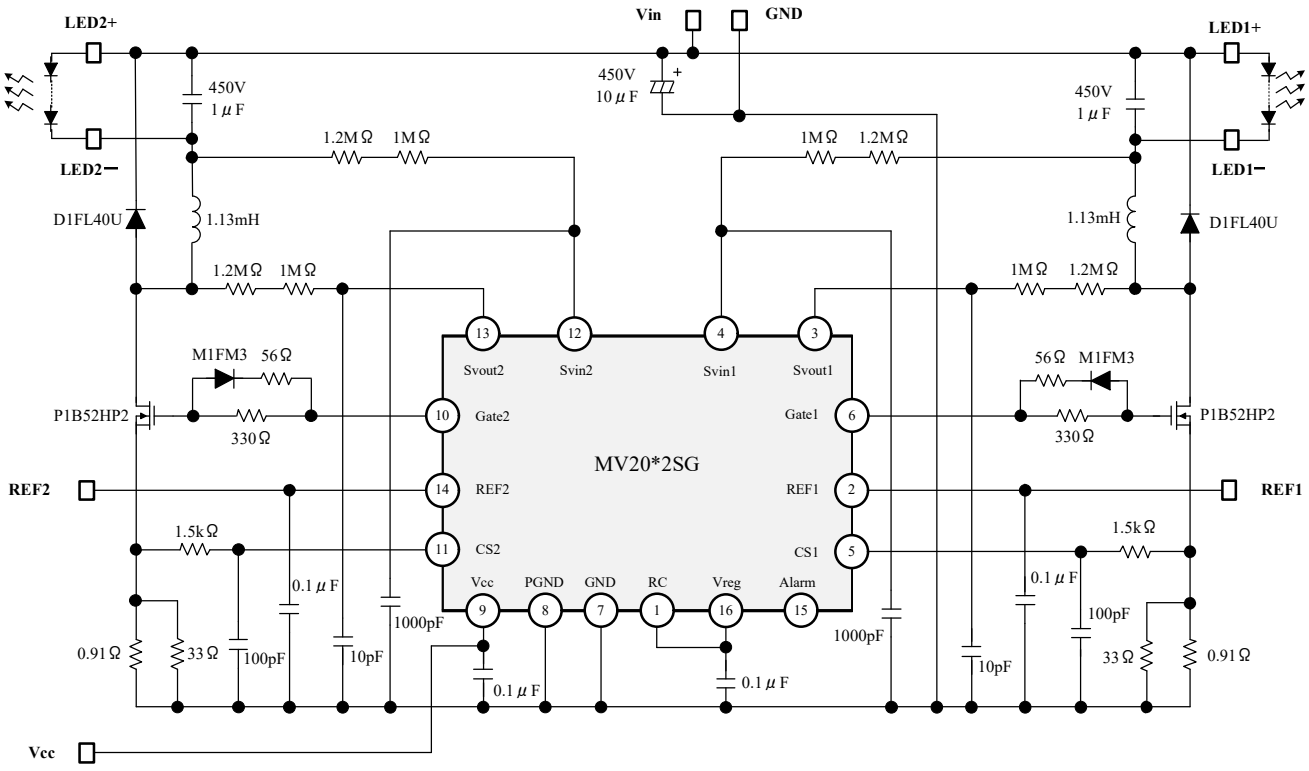
7.1 Power supply specifications and circuit diagram

◆ Power supply specifications

	Min	Typ	Max	Unit
Input voltage (DC)		270		V
Channel 1 output voltage		140		V
Channel 2 output voltage		140		V
Channel 1 output current	0.1 (*1)	300 (*2)	326 (*3)	mA
Channel 2 output current	0.1 (*1)	300 (*2)	326 (*3)	mA

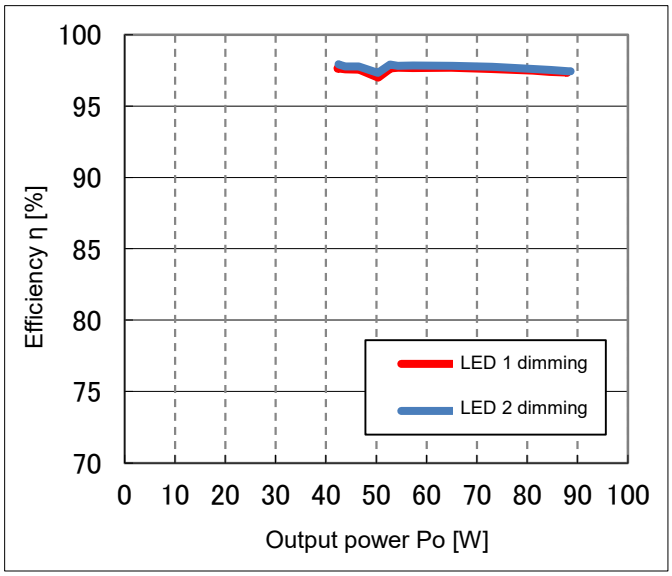
(*1) When Vin = 270 V DC, Vo = 140 V, V_{REF} = 0 V
(*2) When V_{REF} = 2.7 V
(*3) When V_{REF} ≥ 3.3 V

◆ Circuit diagram

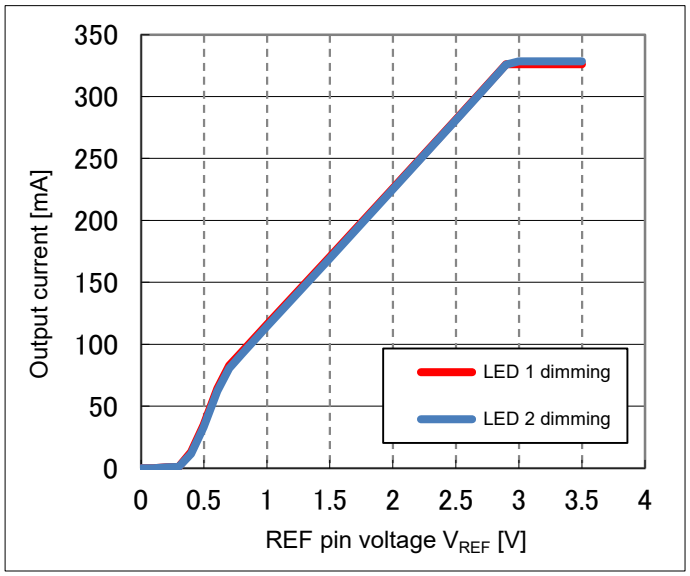


7.2 Power supply characteristics

◆ Efficiency characteristics
(Vin = 270 V DC, Vcc = 14 V, Ireg = 0 A)
Single-channel dimming (V_{REF} fixed at 2.7 V for the other channel)

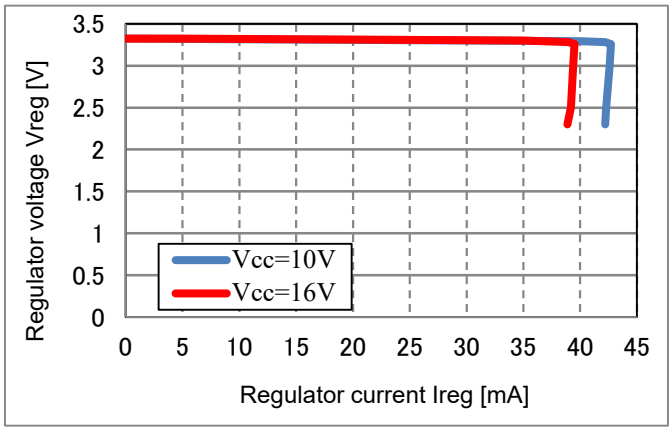


◆ Dimming characteristics
(Vin = 270 V DC, Vcc = 14 V, Ireg = 0 A)
Single-channel dimming (V_{REF} fixed at 2.7 V for the other channel)

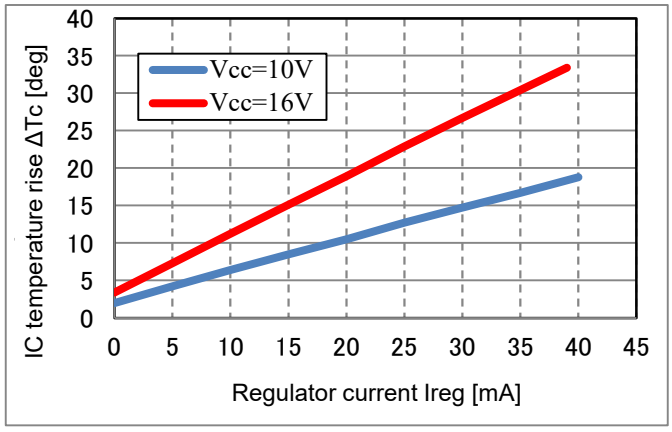


◆ Regulator characteristics (Ta = 25 °C, V_{REF1} = V_{REF2} = 0 V)

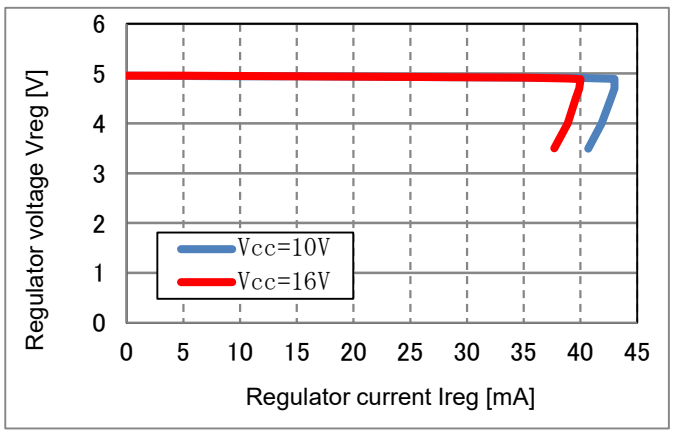
・MV2002SG regulator voltage against regulator current



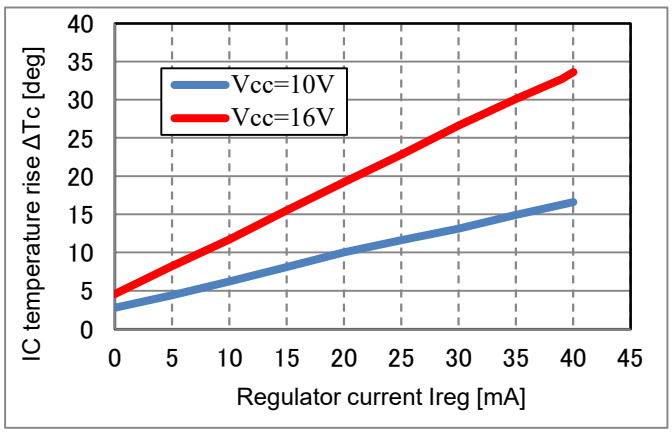
・MV2002SG IC temperature rise against regulator current



・MV2052SG regulator voltage against regulator current

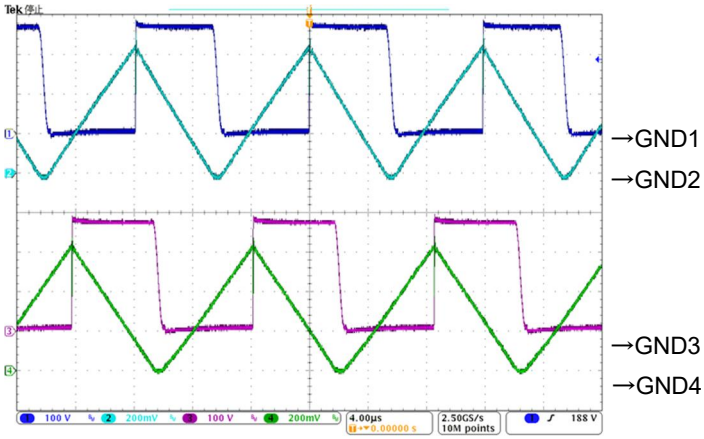


・MV2052SG IC temperature rise against regulator current



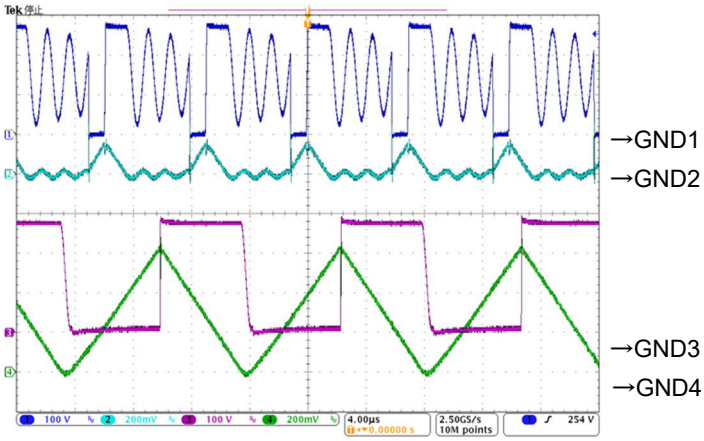
7.3 Operation waveform examples

[A] Frequency modulation region waveform



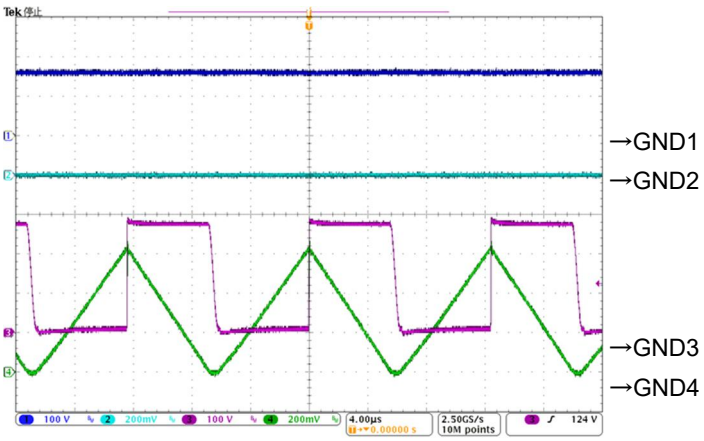
CH1	VDS1	100 V/div
CH2	IL1	0.2 A/div
CH3	VDS2	100 V/div
CH4	IL2	0.2 A/div
time	4 μs/div	
Vin	270 VDC	
Io1	300 mA	
Io2	300 mA	
Channel 1: Dimming 100 % Channel 2: Dimming 100 %		

[B] Off-time modulation region waveform



CH1	VDS1	100 V/div
CH2	IL1	0.2 A/div
CH3	VDS2	100 V/div
CH4	IL2	0.2 A/div
time	4 μs/div	
Vin	270 VDC	
Io1	30 mA	
Io2	300 mA	
Channel 1: Dimming 10 % Channel 2: Dimming 100 %		

[C] Oscillation stop region waveform



CH1	VDS1	100 V/div
CH2	IL1	0.2 A/div
CH3	VDS2	100 V/div
CH4	IL2	0.2 A/div
time	4 μs/div	
Vin	270 VDC	
Io1	0.13 mA	
Io2	300 mA	
Channel 1: Oscillation stopped Channel 2: Dimming 100 %		

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