CAT.No.1K0301-4E

MF2003SV

APPLICATION NOTE
Ver.1.4

Ideal Diode IC
V-Diode™

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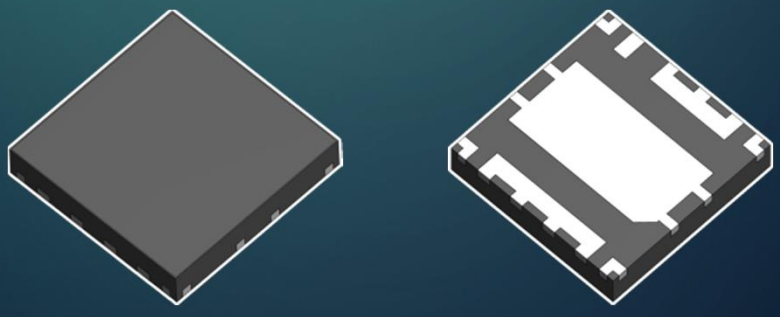

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Contents

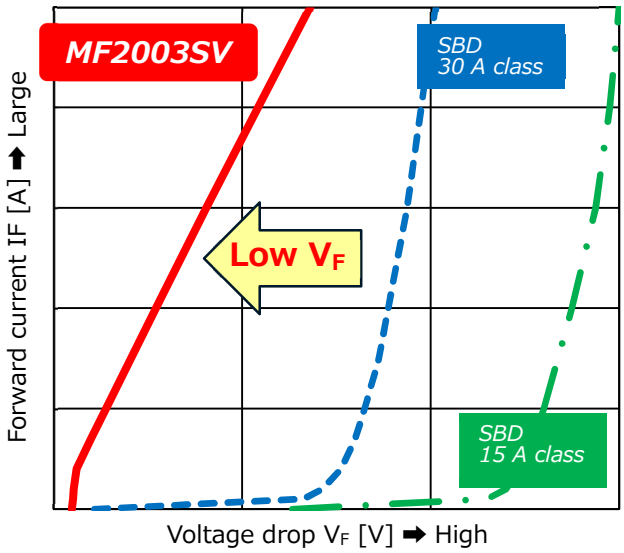
1. Overview

With advances in electronic control technology used in vehicle-mounted devices, the number of onboard Electronic Control Units (ECUs) has also increased, with applications growing increasingly diverse. ECUs use battery or DC/DC converter output as their power source, and diodes have traditionally been used as reverse connection protection and reverse current prevention devices in the input unit. However, the increasingly large currents used in multi-functional electronic devices have raised concerns about increased diode voltage drop (V_F) and heat generation, leading to demand for reverse connection protection and reverse current prevention devices that are capable of suppressing voltage drop and heat generation under high current conditions. In response to this market demand, Shindengen has developed and launched the **MF2003SV ideal diode IC (V-Diode™), which features a P-channel (Pch) MOSFET offering low V_F, low losses, and low heat generation, together with an integrated control circuit with reverse connection protection and reverse current prevention functions**.

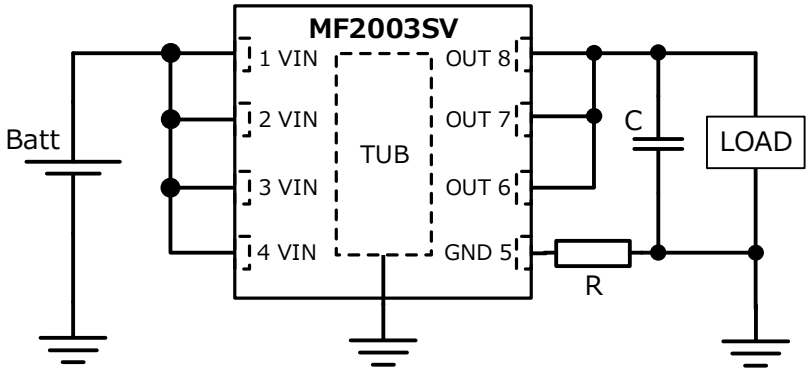
1.1 Features

- Significantly reduced V_F (voltage drop), losses, and heat generation
- Compact leadless package ⇒ Contributes to reduced device size
  WSON8: 4 mm × 4 mm
- Includes integral reverse current prevention and reverse input connection protection functions
- Includes integral ESD protection devices for surge protection at each pin
- Incorporates Pch MOSFET with active clamp function
- Operating voltage: 2.5 V to 40 V
- Rated current: 5 A
- Internal Pch MOSFET ON resistance
  Ron = 53 mΩ (typ), 70 mΩ (max)
- IC consumption current: max. 3 uA
  (*at no load)
- AEC-Q100 compliance (currently undergoing testing)

Example forward characteristics



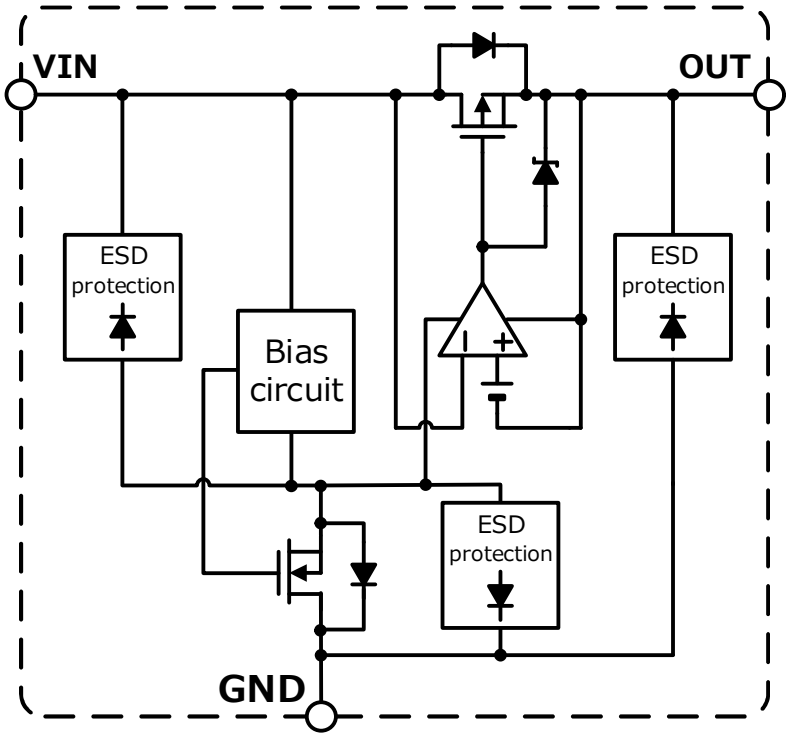
1.2 Typical circuit example



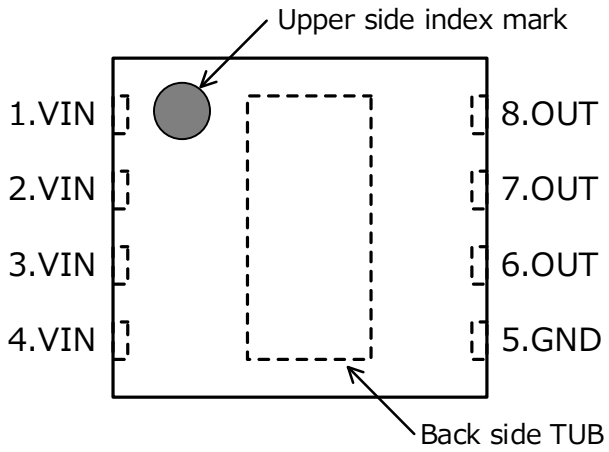
Identical function pins should be short-circuited close to the pins.

The floating and nonfunctional TUB should be used as a pin for heat dissipation. We recommend connecting it to the PCB ground (as in the figure above) or to the MF2003SV GND pin (pin 5). Neither connection affects IC function. The design should consider ways to dissipate heat from the PCB.

1.3 Block diagram



1.4 Pin assignment and pin functions



Package (House Name): WSON8

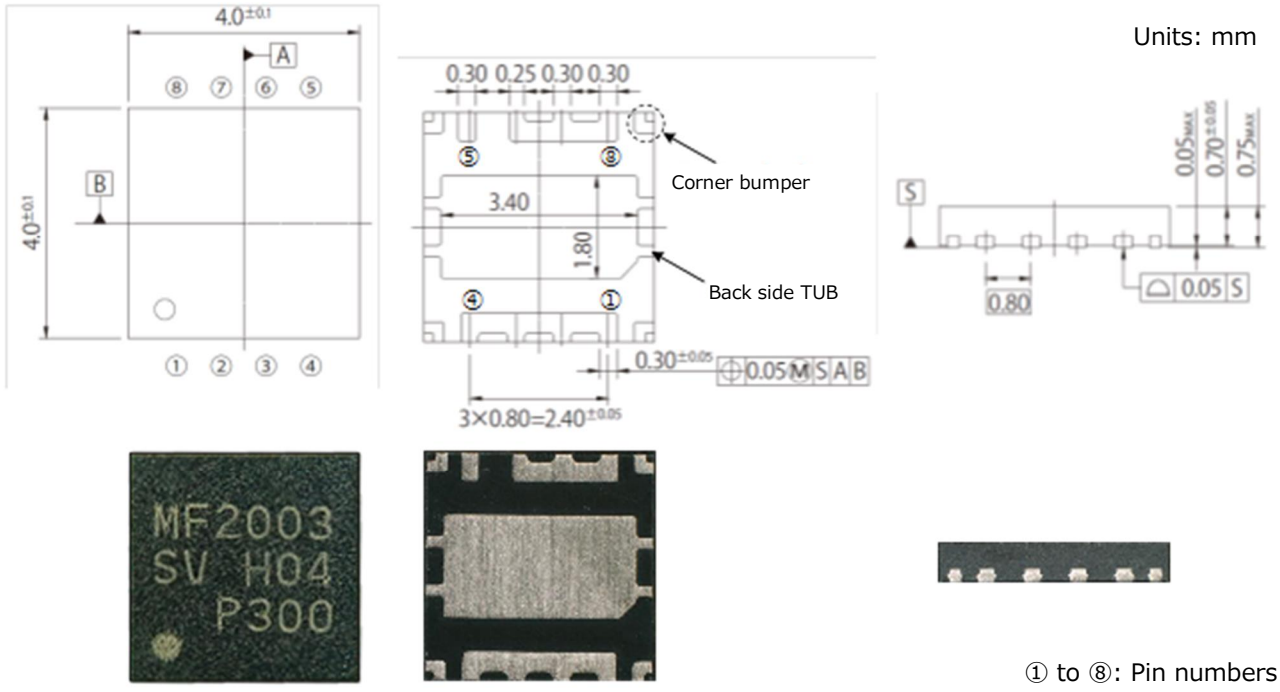
Pin No.	Symbol	Function
1	VIN	Power supply pin
2	VIN	Power supply pin
3	VIN	Power supply pin
4	VIN	Power supply pin
5	GND	Ground pin
6	OUT	Output pin
7	OUT	Output pin
8	OUT	Output pin

* Identical function pins should be short-circuited close to the pins.

The MF2003SV has three different types of functional pins: VIN, GND, and OUT pins. Unlike diodes, three wire connections are required. The IC will not function unless the GND pin is connected. Current will flow through the internal body diode instead of the internal Pch MOSFET. This will not produce the desired ideal diode operation (low voltage drop and low-loss operation). Losses will be large in such cases, and heat generation will increase considerably.

1.5 External appearance and dimensions (WSON8 package)

Units: mm

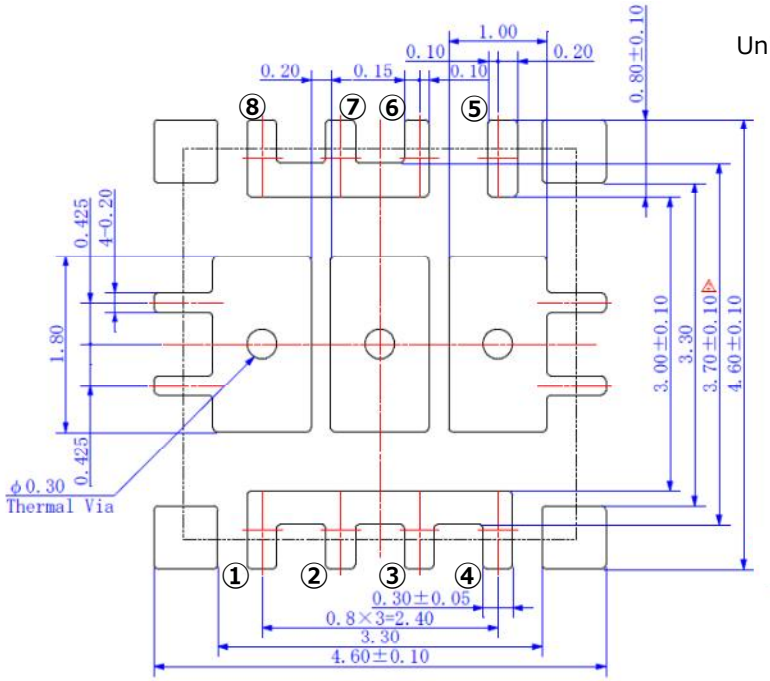


① to ⑧: Pin numbers

The MF2003SV uses a wettable flank package. The solder wetting characteristics can be visually confirmed from the side to allow inspections with visual inspection systems. Fillets are easily created on the side pads to facilitate board mounting. The corner bumpers are provided to ensure consistent soldering performance with respect to thermal expansion during testing. Corner bumpers are floating and have no functions; IC functions will remain unaffected even if the bumpers make contact with adjacent pins or the back side TUB. We recommend arranging the pattern layout while referring to the reference soldering pads shown in the figure below.

1.6 Reference soldering pads

Units: mm



① to ⑧: Pin numbers

2. Specifications

These are reference specifications for the MF2003SV. Please contact Shindengen sales for information on the latest official specifications.

2.1 Absolute maximum ratings

Make sure the absolute maximum ratings are not exceeded when using this IC. IC failure may occur if the absolute maximum ratings are exceeded. Incorporate physical safety measures, such as fuses. It will not be possible to identify the failure mode (open mode or short mode) if the IC fails.

Tj = 25°C (unless otherwise specified)

Item	Symbol	Rating	Units
Input/output ratings			
Supply voltage	V_{VIN}	−42 to 42	V
Output voltage	V_{OUT}	−1.0 to 42	V
Peak repetitive reverse voltage	V_{RRM}	40	V
Average forward current	I_{OUT}	5	A
Surge forward current (*1)	I_{FSM}	70	A
Thermal rating			
Total power dissipation (*2) (*3)	Pd	2.79	W
Junction temperature	Tj	150	°C
Storage temperature	Tstg	−55 to 150	°C
Thermal rating (thermal resistance)			
Thermal resistance (*2) (*3)	Rth(j-a)	43	°C /W
	Rth(j-c)	8.6	°C /W

*1: At 50 Hz, sine wave, non-repetitive, 1 cycle, peak to peak, Tj = 25 °C

*2: For glass epoxy PCB: 114.3 mm × 76.2 mm, thickness 1.6 mm, internal copper foil size: 74.2 mm × 74.2 mm, thickness 35 um

*3: Rating with back side TUB connected. Heat generation should be taken into consideration if the back side TUB soldering is insufficient or if the back side TUB is not connected, as heat dissipation will be reduced.

2.2 Recommended operating conditions

Item	Symbol	Rating	Units
Junction temperature	Tj	−40 to 125	°C

Note: Use outside the range of recommended operating conditions may affect reliability.

2.3 Electrical characteristics

VIN = 12 V, Tj = 25°C (unless otherwise specified)

Item	Symbol	Condition	Rating			Units
			MIN	TYP	MAX	
Main characteristics						
① Quiescent current	Iq	Iout=0A	—	1.8	3.0	uA
② Output leak current	Ioleak	OUT=32V	—	—	10	uA
③ Low level of Logic Input voltage	Ignd	Iout=1A	—	—	300	uA
④ Operating start voltage	Vst	IIN≧0.7uA	—	—	2.5	V
⑤ Regulation voltage	Vds	IIN=10mA	8	25	50	mV
⑥ Delay time of Turn-on	Ton	OUT=0A → −0.5A VIN−OUT＜0.2V	—	5	50	us
⑦ Delay time of Turn-off	Toff	VIN=12V → 0V VIN−OUT＜0V	—	0.5	1.5	us
⑧ Forward voltage	Vbody	IIN=2A, VIN=0V	—	0.8	1.0	V
⑨ MOS RON resistance	Rdson	IIN=2A	—	53	70	mΩ
⑩ Vds voltage during active clamp operation	Vcl	OUT=0V Iout=2A	35	40	46	V

《Explanation of main characteristics》

① Quiescent current (Iq): Consumption current for IC under no load

② Output leak current (Ioleak): Consumption current for IC during reverse current protection operation; value when active clamp is not operating

③ Low level of Logic Input voltage (Ignd): Internal MOSFET gate drawing-out current and consumption current to GND pin.

④ Operating start voltage (Vst): VIN voltage starting IC operation (able to turn on internal MOSFET)

⑤ Regulation voltage (Vds): Voltage setting across VIN and OUT for a light load (0.1 mA ≤ IIN ≤ 10 mA) (Vds value for internal Pch MOSFET); for light loads, the internal Pch MOSFET gate and Vds voltage are controlled to maintain this value

⑥ Delay time of Turn-on (Ton): Delay until the Pch MOSFET turns on when the load increases, corresponding to the time for which current flows via the internal diode; Max value is the value with an external ground pin resistance (10 kΩ) added.

⑦ Delay time of Turn-off (Toff): Delay until the Pch MOSFET turns off after VIN < OUT

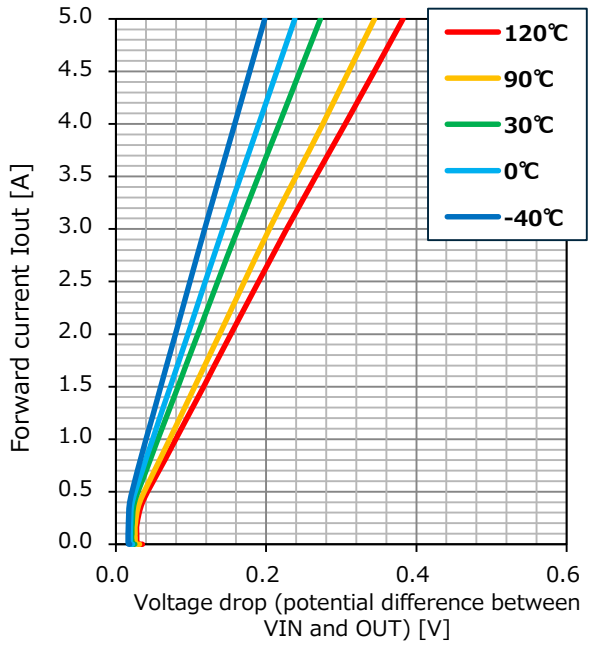
⑧ Forward voltage (Vbody): Voltage across VIN and OUT when current flows via the diode while the MOSFET is off

⑨ MOS RON resistance (Rdson): Resistance when internal Pch MOSFET is on (@ load current = 2 A)

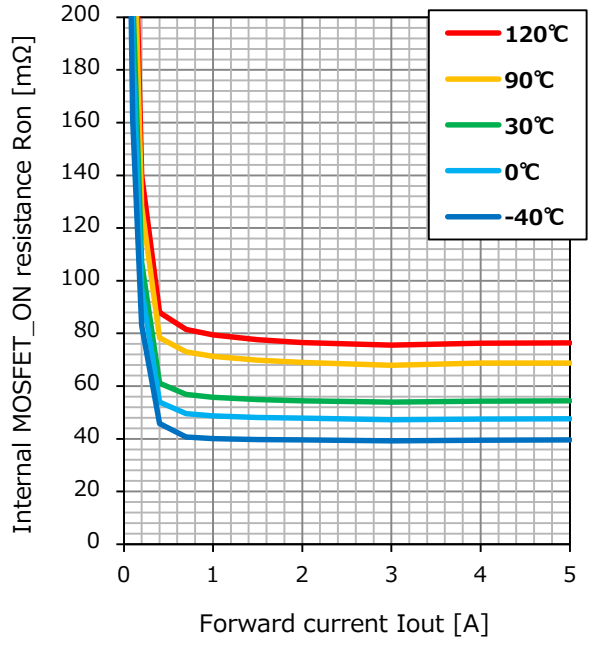
⑩ Vds voltage during active clamp operation (Vcl): Vds voltage when the active clamp function starts to operate; Vds voltage will be clamped by the active clamp if the VIN pins are subject to a voltage surge due to sudden input fluctuations. This clamp function protects the IC against surges at the VIN pins.

2.4 Reference characteristics

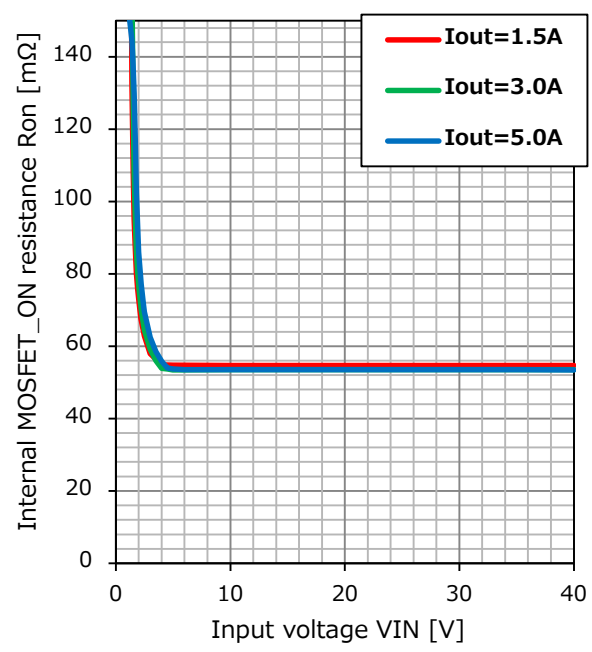
The main characteristics diagrams are shown here. This data is for reference purposes and does not constitute a guarantee. The temperature indicated is the case temperature Tc.



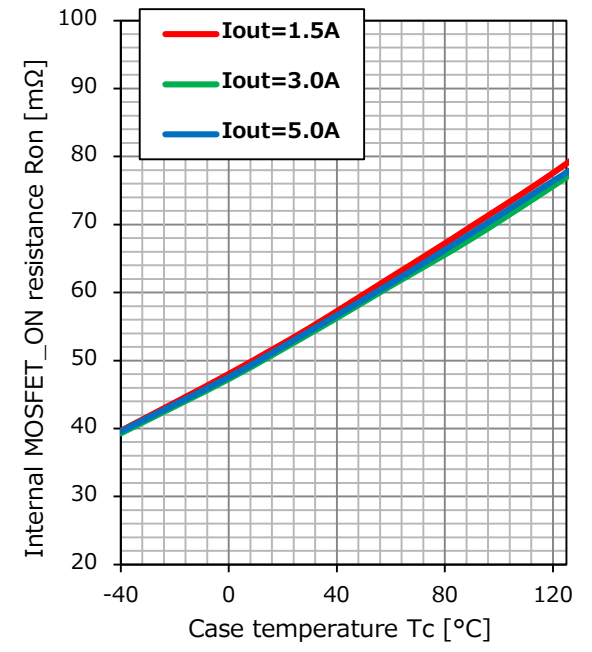
Reference characteristic diagram 1:
Forward characteristics



Reference characteristic diagram 2:
Resistance current characteristics



Reference characteristic diagram 3:
Resistance input voltage characteristics



Reference characteristic diagram 4:
Resistance temperature characteristics

3. Circuit Operations and Functions

3.1 Basic operation

The MF2003SV is a device that incorporates a Pch MOSFET and control circuit to ensure low-loss diode operation (ideal diode operation). It allows current flow in the forward direction (from Batt to LOAD) while preventing current flow in the reverse direction (from LOAD to Batt), as shown in the figure on the right.

The comparator inside the control circuit compares the VIN and OUT voltages and turns the Pch MOSFET gate on or off to establish or shut off the connection between Batt and LOAD.

- Batt > LOAD: The potential difference (Vgs) between the gate and source is increased to turn on the Pch MOSFET and establish the connection between VIN and OUT.
- Batt < LOAD: The potential difference (Vgs) between the gate and source is reduced to turn off the Pch MOSFET.

For more information, refer to Section 3.4 “Reverse current prevention function” on page 10.

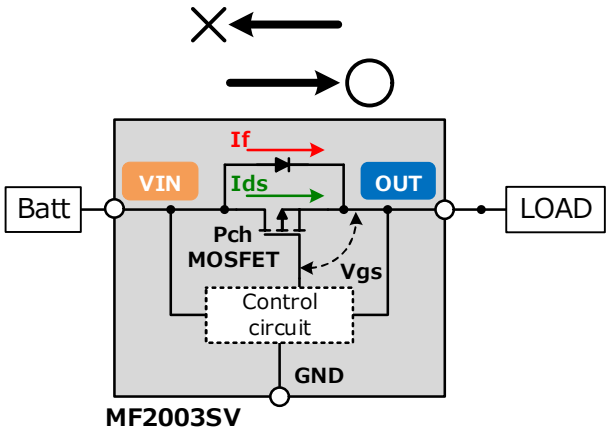


Fig. 1 MF2003SV schematic diagram

3.2 Startup, input drop, and shutdown operations

When VIN is applied, a current (If) flows through the body diode and is fed to OUT until VIN reaches the startup voltage Vst = 1.9 V (typ). When VIN reaches the startup voltage Vst = 1.9 V, the Pch MOSFET turns on, and a current (Ids) flows through the Pch MOSFET to feed OUT. Note that, during startup, even with no load (LOAD = 0 A), current must flow from the VIN pins to the OUT pins to charge the output capacitance (capacitor on the OUT side).

If there is no load after startup, the Pch MOSFET gate voltage and Vds voltage are controlled by the control circuit in the IC to set the voltage between VIN and OUT to the VIN - OUT regulation voltage Vds = 25 mV (typ). Even if the input voltage (VIN) drops during operation, provided it remains within the IC operating voltage range (2.5 V to 40 V), the IC will continue to operate, minimizing the OUT output drop.

When VIN decreases during shutdown, the reverse current prevention function activates to turn off the Pch MOSFET (refer to Section 3.4 “Reverse current prevention function” on page 10), interrupting the current supply from the device. Since the capacitor connected to the OUT pins is sufficiently charged at this point, the OUT voltage gradually decreases as the load current is still being supplied from the capacitor.

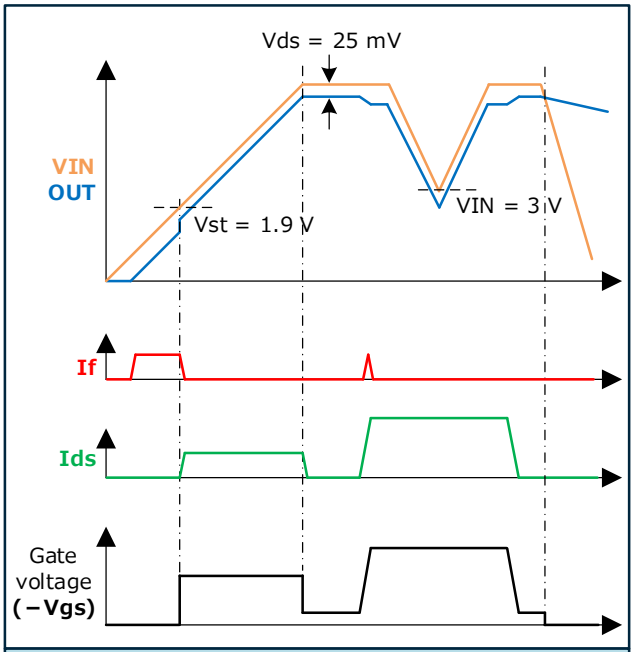


Fig. 2 Startup, input drop, and shutdown operations

3.3 Load fluctuations

As mentioned on the previous page, during no-load conditions, the voltage between VIN and OUT is set to 25 mV.

If the load current increases suddenly, the current (If) is fed to the OUT pins via the body diode until the Pch MOSFET is turned on driven by the Pch MOSFET gate. As current flows through the diode here, the voltage between VIN and OUT rises to the forward operating voltage for the diode, Vbody = 0.8 V (typ). The time from the point at which the load fluctuates suddenly until the Pch MOSFET turns on is the turn-on delay time, Ton = 5 us (typ). While the Pch MOSFET is on, a load current (Ids) is fed via the Pch MOSFET. If the load is fed through Ids, there will be no current (If) flowing through the diode, and so Iload will be equal to Ids. The voltage between VIN and OUT is "Ids×Ron", and since Ron > 25 mΩ while the PchMOSFET is on, VIN-OUT=Ids×Ron > 25mV.

If the load current decreases suddenly, the gate and Vds voltages are controlled to ensure that the voltage between VIN and OUT is kept at 25 mV.

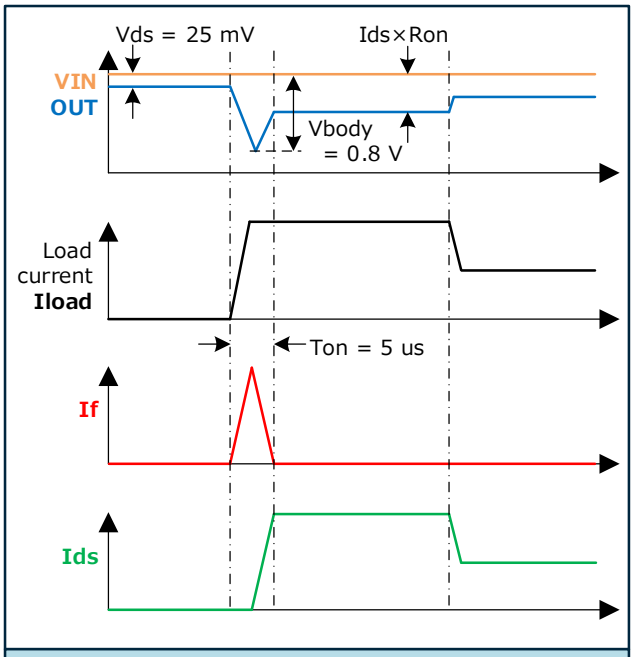


Fig. 3 Load fluctuation operation

3.4 Reverse current prevention function

If VIN decreases so that VIN < (OUT + 25 mV), the reverse current prevention comparator operates to turn off the Pch MOSFET and prevent reverse current flow (see Figure 4). The current (Ids) in the Pch MOSFET continues to flow until the gate voltage reaches 0 V. The time from the point at which the reverse current is detected until the Pch MOSFET turns off is the turn-off delay time Toff. The output continues to be supplied during this time with current from the capacitor.

When VIN is restored, the load current is supplied via the internal diode (If) until the Pch MOSFET is turned on by the gate drive. When the Pch MOSFET turns on subsequently, the load current is supplied via the Pch MOSFET (Ids).

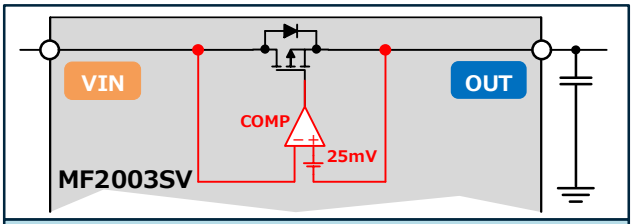


Fig. 4 Reverse current prevention comparator

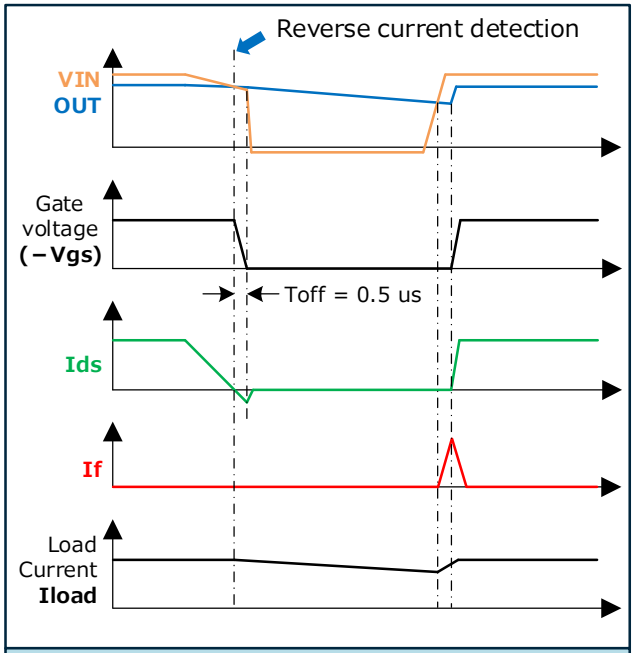


Fig. 5 Reverse current prevention operation

3.5 Operation for input reverse connection

The MF2003SV features an input reverse connection protection function.

3.5.1 Pch MOSFET gate control for input reverse connection

When the input is connected in reverse, current flows inside the MF2003SV from the GND pin in the direction indicated by the purple arrow in the diagram to control the internal Pch MOSFET gate. This causes the Pch MOSFET Vgs potential to become positive, and the Pch MOSFET turns off. Even if VIN is suddenly subjected to a reverse voltage, for example, the control circuit controls the gate to turn off the Pch MOSFET and ensure that it is not turned on by the gate due to the capacitance between VIN and OUT (e.g., the internal Pch MOSFET gate-to-source capacitance and gate-to-drain capacitance).

Even if the internal Pch MOSFET were to turn on while the input connection is reversed, the ESD protection device between the OUT and GND pins limits the negative voltage at the OUT pins, thereby limiting the negative voltage at the load side. Note that, when the input connection is reversed, a small leakage current flows from the OUT pins in the form of the output leakage current Ioleak with a maximum value of 10 uA.

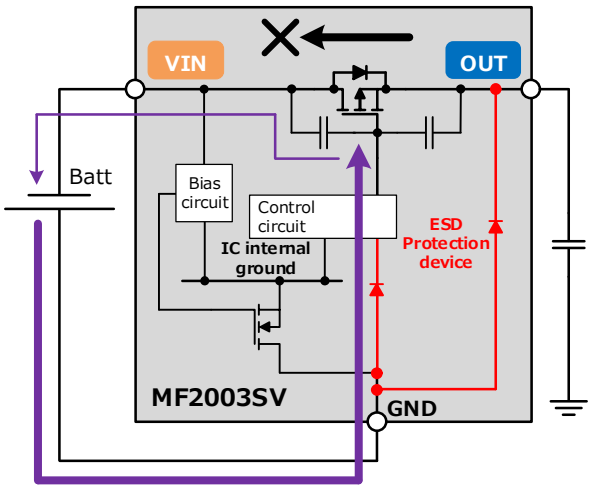


Fig. 6 Input reverse connection protection schematic diagram

3.5.2 IC protection for input reverse connection

The MF2003SV features a function to protect the IC itself from reverse input connection. Since a three-wire connection is used for an ideal diode circuit configuration, reversing the input connection polarity can create issues such as large currents flowing in the IC from the GND pin to the VIN pins, which can damage the IC (as shown on the left in Figure 7). To prevent damage to the IC due to reverse input connection, the MF2003SV incorporates a reverse connection protection MOSFET between the GND pin and IC internal ground (as shown on the right in Figure 7). The reverse connection protection MOSFET is off when input is connected in reverse, preventing current from flowing from the GND pin to the VIN pins and preventing short-circuiting of the battery between VIN and GND. The GND pin and IC internal ground are also isolated; the IC is not powered, preventing the control circuit from operating and preventing the internal Pch MOSFET from being turned on unintentionally.

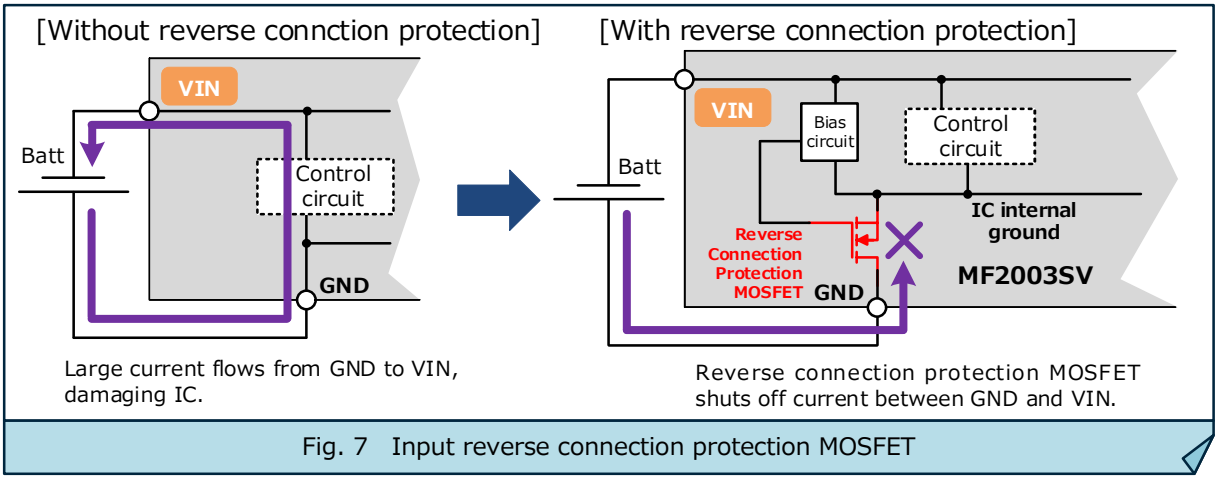


Fig. 7 Input reverse connection protection MOSFET

3.6 Internal protection devices and active clamp function

The MF2003SV features surge protection devices for each pin to protect the IC itself.

3.6.1 Overview of internal surge protection devices

The MF2003SV includes ESD protection devices for each functional pin to protect against surges.

A Zener diode is included to protect the internal Pch MOSFET gate against spike noise when the load is inductive.

An active clamp function is provided (as shown in the figure on the right) to protect the internal Pch MOSFET Vds against surge voltages caused by sudden fluctuations on the input side.

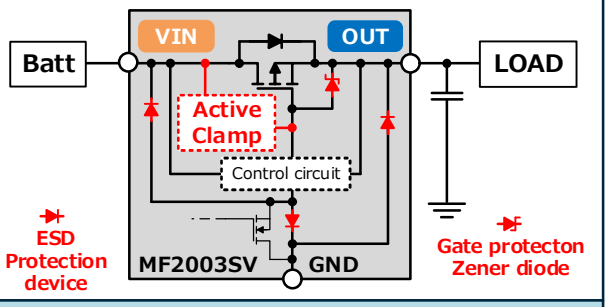


Fig. 8 Schematic of MF2003SV internal surge protection device

3.6.2 Active clamp function operation

If a high-frequency negative surge pulse is applied to the VIN pins, the active clamp function is triggered when the Pch MOSFET Vds voltage (voltage between OUT and VIN) reaches the active clamp operating voltage Vcl = 40 V (typ). Clamping the internal Pch MOSFET Vds voltage keeps it from exceeding the Pch MOSFET Vds voltage limit. Since the capacitor connected to the OUT pins is sufficiently charged at this point, fluctuations (drops) are minimal at the OUT pins, and once Vds drops to 40 V or less, clamping by the active clamp function is canceled.

Note that active clamping acts as a surge absorption function, and is not intended for constant voltage purposes. Make sure the voltage between OUT and VIN does not exceed the Vds voltage Vcl = 35 V (min).

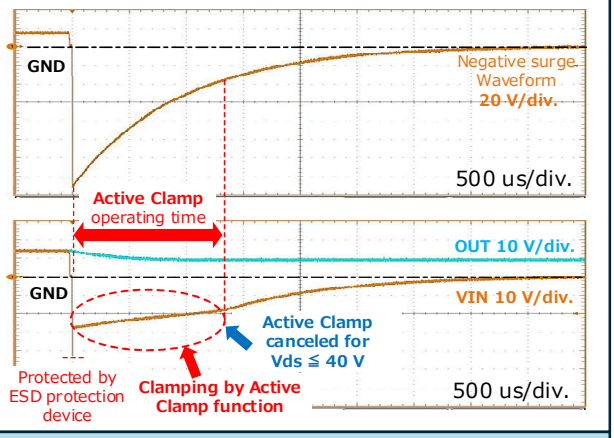


Fig. 9 Active clamp operation example

3.7 IC consumption current

The IC consumption current for the MF2003SV varies according to the operating conditions, as shown in the figure on the right. The IC consumption current (also known as the dark current) for no-load conditions is limited to Iq = 3 uA (max) by the IC internal bias circuit and control circuit.

Under normal operating conditions, as the internal Pch MOSFET gate is controlled in the on-state, the operating consumption current is Ignd = 300 uA (max); in reverse current or reverse connection protection operation, the IC power consumption is limited to the output leakage current Ioleak = 10 uA (max).

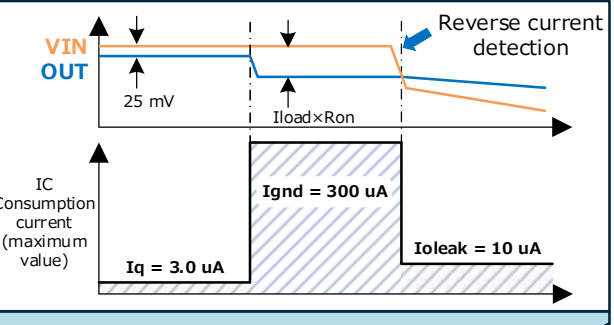


Fig. 10 IC consumption current

4. Peripheral Component Selection

The selection criteria described in this document are provided solely for guidance. Always evaluate the actual installation before determining parameters.

4.1 GND pin resistor

The MF2003SV uses WSON8, with OUT pin (pin 6) and GND pin (pin 5) positioned side by side. If adjacent pins are short-circuited (between OUT and GND pins), excessive current may flow into the MF2003SV and cause it to fail. We recommend adding **a GND pin resistor as an abnormality countermeasure to prevent damage to the MF2003SV by limiting the excessive current flowing into the MF2003SV if adjacent pins were to be short-circuited**.

Since the GND pin resistor is intended to limit excessive current to the MF2003SV, this is not required if excessive current can be limited by placing a fuse or other similar component on the input (VIN) line.

4.1.1 GND pin resistor R1 selection

The recommended design range for the GND pin resistor R1 is 1 kΩ to 10 kΩ. When selecting the R1 resistance value, determine the power and size of the resistance by calculating the allowable power value (P) using the following equation:

$$\frac{(VIN-Vbody)^2}{R1} \leqq P$$

VIN: Maximum power supply voltage, Vbody: Body diode forward voltage

Calculate using Vbody = 0 V to obtain the maximum power when calculating allowable power for the resistance.

Refer to the following table for the effects of the GND pin resistor R1 on ideal diode circuit operations:

R1 resistance value	High	—	Low
① Resistance size taking into account short-circuiting between adjacent pins (allowable capacity for resistance components)	Small	⇔	Large
② Delay time of Turn-on	Long	⇔	Short

For ①, increasing the R1 resistance value reduces the allowable power for the resistance in accordance with the equation provided on this page, enabling the resistance size to also be reduced.

For more information on ② Delay time of Turn-on, refer to the next page.

4.1.2 Turn-on operation with addition of GND pin resistor

With the MF2003SV, during normal operation, the gate drawing-out current flows to the GND pin as indicated by the purple arrow in the figure on the right.

Adding a GND pin resistor limits the gate drawing-out current, increasing the time for which the internal Pch MOSFET is turned on, which also affects the turn-on time, Ton (see Figure 12). If the resistance is high, the turn-on delay time, Ton, will increase during sudden load fluctuations and other events, slowing the turn-on response. As a guideline, we recommend a resistance that does not exceed 10 kΩ to ensure it does not exceed twice the original capability of the IC (at 0 kΩ) (see Figure 13).

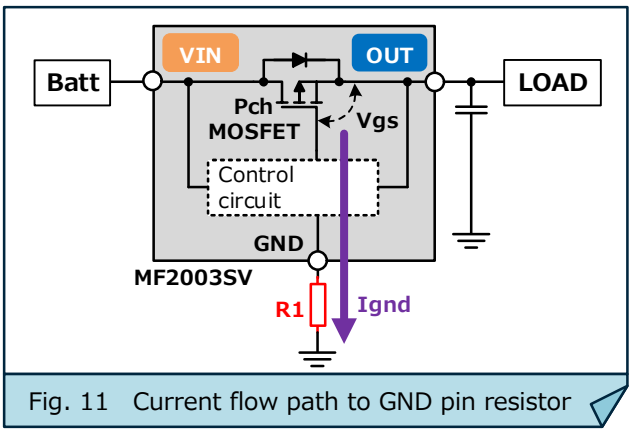


Fig. 11 Current flow path to GND pin resistor

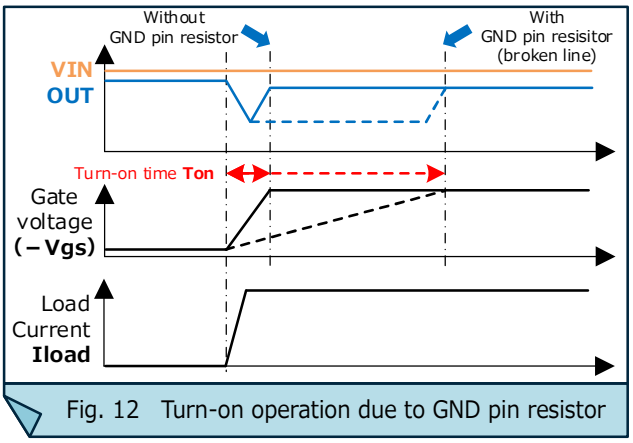


Fig. 12 Turn-on operation due to GND pin resistor

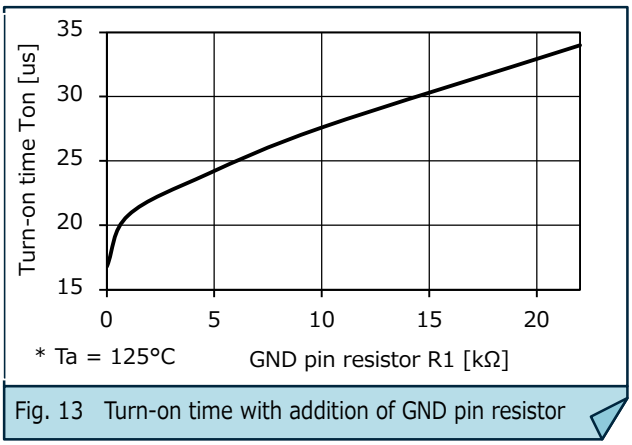


Fig. 13 Turn-on time with addition of GND pin resistor

<Issues created by increased delay time of turn-on >

1) Heat generation during turn-on operation

During the turn-on operation, load current is fed via the internal body diode (see Figure 12). Heat generation with the MF2003SV during high-frequency operation with repeated turn-on poses special concerns. The graph in Figure 13 shows the turn-on time for an ambient temperature Ta = 125°C (worst temperature condition).

2) Operation via body diode only

If the turn-on time becomes excessively long, the internal Pch MOSFET turn-on will be delayed. If an AC voltage is superimposed on the input, the operation time for which current flows through the internal body diode is increased, significantly increasing losses for the MF2003SV. Thus, the recommended upper limit for the resistance is set to 10 kΩ.

As described above, increasing the delay time of turn-on creates issues of heat generation with the MF2003SV. This will vary depending on the board heat dissipation conditions, so the actual installation should be evaluated before determining the parameters.

4.2 Capacitors closed to the pins

The MF2003SV uses the potential difference across VIN and OUT to determine operations. To prevent operation when VIN < OUT during steady-state and **to ensure that the IC OUT pins and GND are not affected**, we recommend **adding a capacitor (e.g., ceramic capacitor) of 1 uF or more to the OUT pins (between OUT and GND)**. Place this capacitor as close to the IC as possible. The input-side capacitor Cin (between VIN and GND) is not required if VIN and OUT are stable due to the addition of the output capacitor C1. If noise enters the VIN pin from the battery side, reverse current detection may activate during steady-state and cause the product to stop. To stabilize VIN, we recommend adding a noise suppression capacitor C3 of 0.1uF or less (sufficiently smaller than C1 = 1uF) close to the VIN pin.

The inrush current during startup can also become significant if the capacitor C2 (output capacitance component) added to the output line is large and the output-side impedance is low. Check the actual installation before selecting components to ensure that the current does not exceed the surge forward current I_{FSM} rating of 70 A for the IC (maximum allowable peak current for a 10 ms pulse width sine wave).

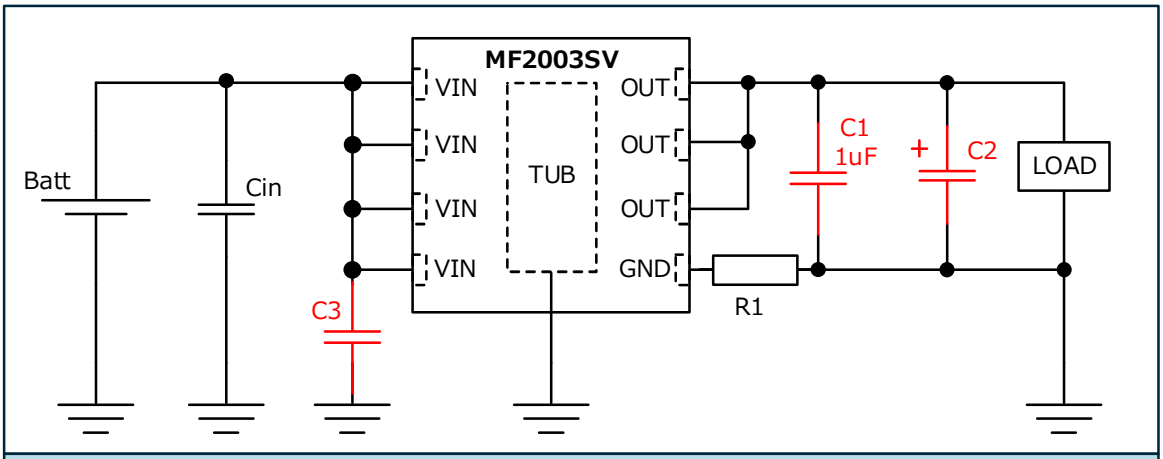


Fig. 14 capacitors close to the pins

* I_{FSM} reference:

The inrush current peak value and applied pulse width vary depending on the capacitance of capacitor C2. Figure 15 shows the reference IFSM tolerance for sine wave peak current with a pulse width in the range 1 ms to 100 ms. This data is provided solely for reference purposes and does not constitute a guarantee.

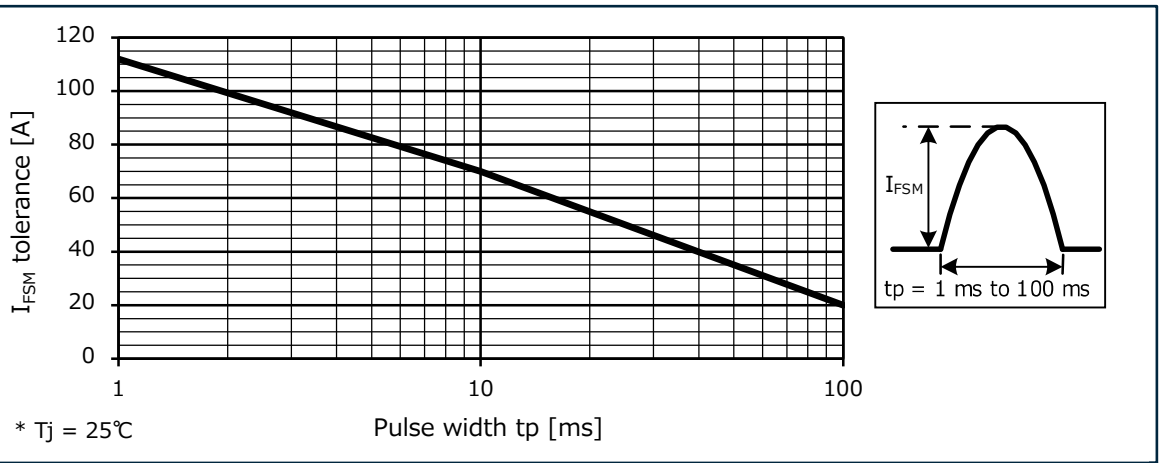


Fig. 15 Reference I_{FSM} tolerance for sine wave peak current with a pulse width 1 ms to 100 ms

5. Example Application Circuits

This section provides examples of circuits using the MF2003SV. Regard these as reference circuit examples.

5.1 ORing connection

This example shows an ORing connection using MF2003SV ICs for separate power supplies, Batt1 and Batt2 (redundant power supply system). Even if one battery power supply is disconnected, output can be maintained from the other power supply circuit.

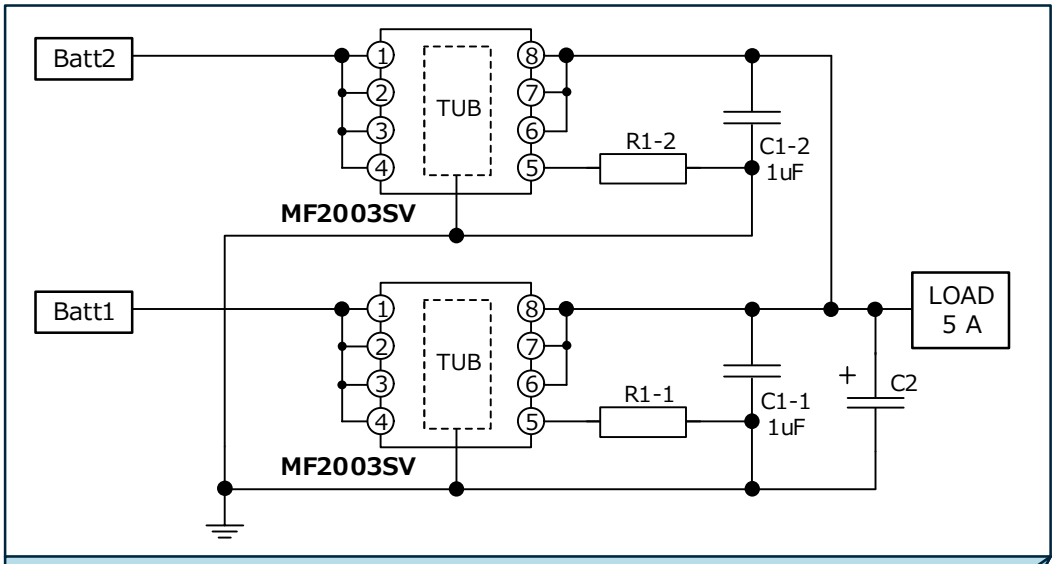


Fig. 16 ORing connection

5.2 Parallel connection

MF2003SV ICs can be used in parallel, as shown in the circuit below, to handle currents of 5 A or greater. R1-1 and R1-2 must have the same resistance, as imbalances in power loss and heat generation will occur during turn-on if delay times differ.

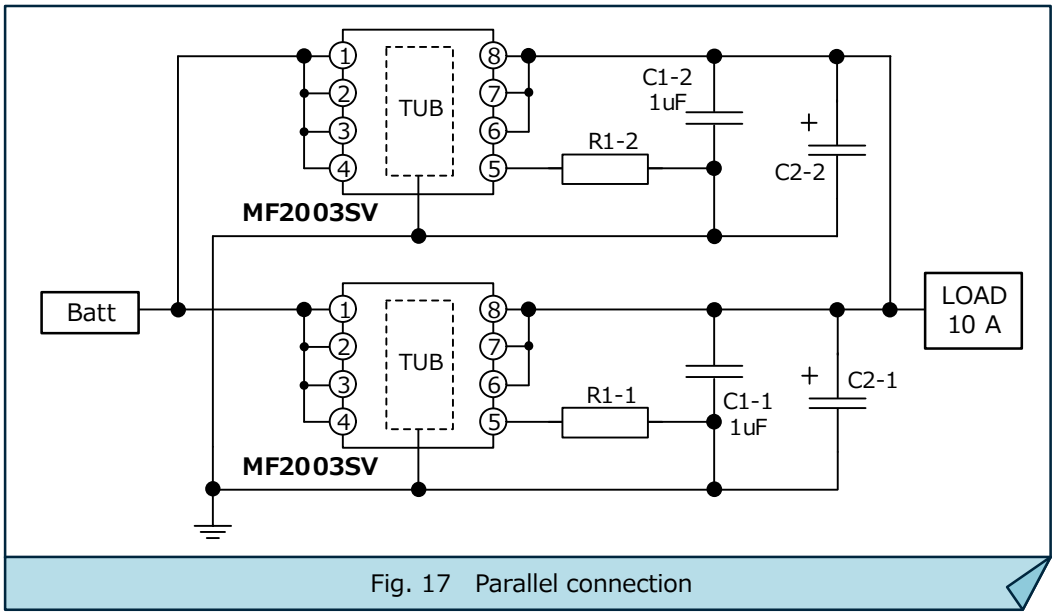


Fig. 17 Parallel connection

5.3 Input surge protection

Design the installation to ensure that the voltage applied to the VIN pins of the MF2003SV is within the rated range of -42 V to 42 V. If the VIN pins are subjected to high-frequency surges exceeding this rating, we recommend adding a Shindengen bidirectional TVS, as shown in the circuit below (ZD1).

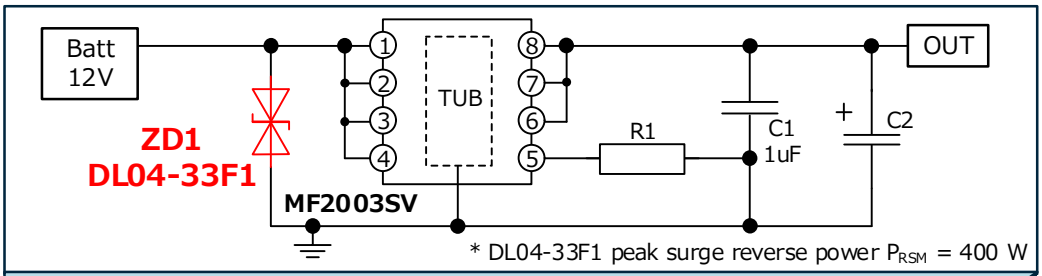


Fig. 18 Input high-frequency surge protection

If load dump protection is required, add a high-surge-capacity TVS, as shown in the circuit below (ZD2).

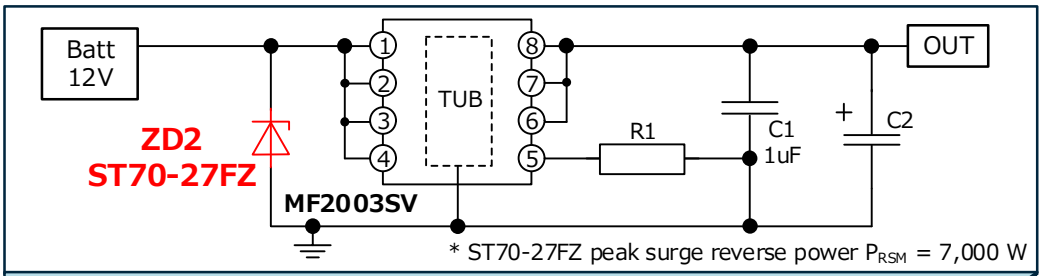


Fig. 19 Load dump protection

Note that the TVS heat generation will vary depending on the thermal performance of the installation board. Be sure to check operation on the actual installation before determining the parameters.

5.4 Negative output voltage protection

If protection is required against ringing on the load side when an inductive load is connected or against negative output voltage due to output leakage current when the input is reversed, a Schottky barrier diode (D1) can be added, as shown in the circuit below, to limit the output (LOAD voltage) from becoming negative.

In the circuit with D1 added, during normal operation when VIN > GND, a leakage current occurs in the direction from the cathode to the anode of D1. To minimize the no-load current consumption (dark current), select a diode with a small reverse current, I_R.

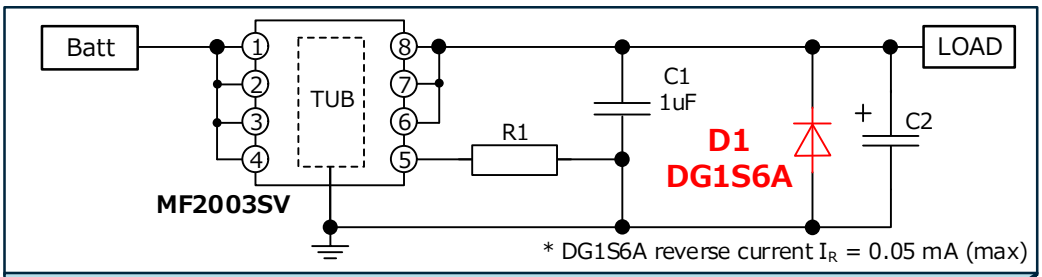


Fig. 20 Negative output voltage protection

6. Pattern Layout

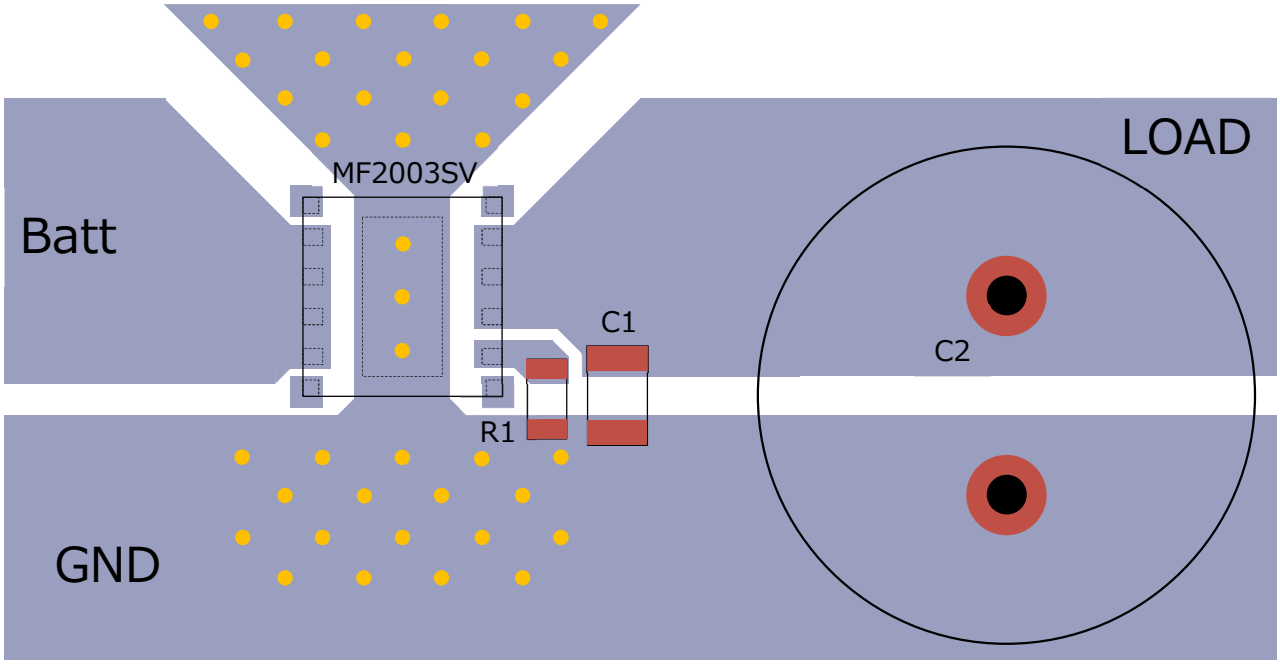
This section describes the precautions required for pattern design. Be sure to check operation on the actual installation before determining the layout.

Note the following four points during pattern design:

1. The MF2003SV includes reference soldering pads (see page 5). These do not guarantee soldering results after the PCB is mounted. Aside from the soldering pad pattern, soldering is affected by factors such as the solder used, solder quantity (printed mask thickness and mask opening size), flux used, soldering pads (including the surrounding area of this IC product), and solder melting temperature profile. The actual installation must therefore be checked through testing before commencing production.
2. As with other power devices, the MF2003SV may suffer significant heat generation leading to failure if the heat generated during operation cannot be efficiently dissipated. A heat-dissipating pattern such as an back side TUB must be installed to efficiently dissipate heat. Factors such as the size of the heat-dissipating pattern and the thickness (thermal conductivity) of the substrate copper foil must be appropriately designed taking into account the operating environment, as they determine the effective power dissipation.
3. When arranging the peripheral components, place the capacitors and GND pin resistors as close to the IC as possible.
4. Design power lines carrying large currents to be as wide and as short as possible. Separate the GND line into the power GND and IC GND and connect the IC GND to a stable potential with minimal current fluctuation.

6.1 Example pattern layout

This example shows a pattern layout with a double-sided board. (● are thermal vias.)



MF2003SV
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SHINDENGEN ELECTRIC
MANUFACTURING CO., LTD.