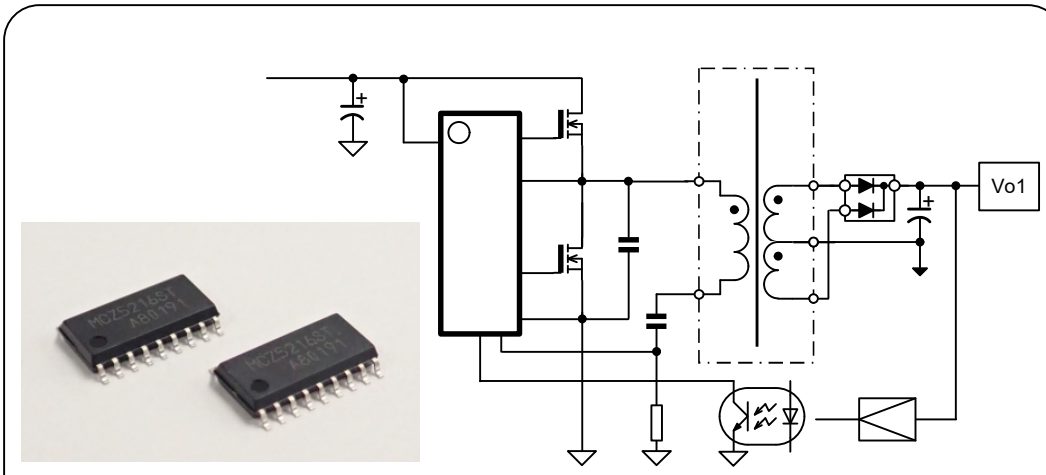
Standby with X-cap discharge function LLC power supply resonant bridge converter control IC

MCZ5216ST



Application Note ver. 1.0

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1 : General Discription	
1.1: Features	**4**
1.2: Internal Block Diagram	**5**
1.3: Pin Assignment	**6**
1.4: Function List for each Pin	**6**
2 : Discription of Basic Operation	
2.1: Control Method of each Operation	
2.1.1: Input-Output Detection Mode	**7**
2.1.2: Oscillator Control Method and operation Mode	**8**
2.1.3: HV startup	**9**
2.2: AC Input/Output Voltage Detection Mode	
2.2.1: Power Supply(AC Input/Output Detection Mode)	**11**
2.2.2: X Cap discharge / Input voltage detection (LS, Vsen Terminals)	**12**
2.3: DC Input Voltage Detection Mode Operation	
2.3.1: Power Supply(DC Input Detection Mode)	**13**
2.4: Each Mode common Terminal Operation	
2.4.1: Gate Driver Output(VGL and VGH terminals)	**15**
2.4.2: Oscillation Control (FB terminal)	**16**
2.4.3: Over-Current-Protection (CS and CSO terminal)	**18**
2.4.4: Input Voltage Correction of OCP2 (CS terminal)	**22**
2.4.5: Soft-Start, di/dt Protection at startup, Latch-Stop (SST pin)	**24**
2.4.6: High-Side-Driver Power Supply(VB terminal)	**27**
2.4.7: Light-Load-Area-loss Improvement(ASTBY, Burst terminal)	**27**
2.4.7.1 : Active Standby Function	**28**
2.4.7.2 : Burst Function	**31**
2.4.8: Thermal shutdown Protection(TSD function)	**33**
2.4.9: Over-Voltage-Protection of Vc1 (Vc1 OVP function)	**33**
2.5: Reference	**34**
3 : Peripheral Circuit Constants Setting	
3.1: Input monitoring section design in AC input voltage detection mode (LS, Vsen pin)	**35**
3.2: Input monitor design in DC input voltage detection mode	**37**
3.3: Oscillation Control (FB terminal)	**38**
3.4: Timer charge-time adjustment at soft start and abnormality (SST terminal)	**40**
3.5: Over-Current-Protection (OCP & di/dt), Adjustment (CS & CSO terminal)	**41**
3.6: Circuit Constants Setting when using Active Standby	**42**
3.7: Circuit Constants Setting when using Burst	**42**
4 : Pattern layout of peripheral of IC	
4.1: Caution of pattern layout of peripheral of IC	**44**
5 : Circuit Examples	
5.1: Basic Circuit	**46**
6 :Dimension	
6.1: SOP18 (MCZ5216ST)	**47**

1 General Discription

MCZ5216ST is a frequency modulation type current resonance power supply control IC. Equipped with a high voltage self-start terminal (drain kick function) with a withstand voltage of 600V, enabling lossless start-up. In addition, it has a high-voltage gate driver and can directly drive the high-side MOSFET.

It is realizable that standby power can be further reduced as X-capacitor discharge resistance can be expelled by an X-capacitor discharge function. And equipped with two types of input detection modes enables either AC input or LLC section input after bridge Diode rectification (X capacitor discharge function supports only AC input.)

In addition, various protection functions such as overcurrent protection function and out-of-resonance protection (Capacitive Mode Protection) function are provided, which can reduce the number of components and also can realize high efficiency.

Equipped with standby power improvement function during standby (active standby function, burst function), it is maintainable for the power supply by high efficiency through the entire load range, so it is matched with the following products.

- Power Supply for Large Flat Screen TV like LED/Organic-EL
- Power Supply for OA Equipment like Lasor Printer
- Power Supply for External device like AC Adaptor.
- Industrial Machinery Power Supply.
- Isolated LED Lighting Power Supply.
- Power Supply for Audio, and Projector.

1.1 Feature

1. Equipped with a self-starting terminal of a withstand voltage(600V) , and achieved lossless starting.
2. Built-in 600V withstand voltage gate driver that boasts high reliability, and it enables high-side MOSFET also to drive directly.
3. Equipped with X-capacitor discharge function to reduce discharge resistance loss. ***NEW***
4. Due to equipped with input detection mode for AC & DC, various input voltage detection is possible. ***NEW***
5. Power good signal enables transmission of IC operating status via photocoupler (AC input detection mode) ***NEW***
6. Equipped with various protection functions required for LLC converter (Overcurrent, timer latch, undervoltage, overheat-protection)
7. Equipped with overcurrent protection function by direct detection of resonance current in both positive & negative directions.
8. Equipped with capacitive mode protection function by direct detection of the resonance current in both positive & negative directions.
9. Support a wide range of input voltages by Vc1 withstand voltage (35V).
10. Built-in regulator(Vc2) for MOSFET drive power supply realizes stable drive.
11. Independent low-voltage protection (UVLO) for high-side and low-side gate outputs.
12. Equipped with soft start function to reduce di/dt stress of MOSFET
13. Equipped with a safe protection that stops operation during low-input-voltage operation such as Brown Out.
14. Equipped with an input voltage correction function in the overcurrent protection function of frequency clamp type corresponging to the peak load, the stress can be reduced during over-load by reducing the dependency of the overcurrent protection operation start points due to input voltage.
15. By switching the timer charge current in two stages during OCP2 operation, the protection is achieved during over load and safety operation of several 100ms at peak load.
16. Equipped with an active standby function to improve efficiency at light load.
17. Equipped with a high-efficiency burst function to improve efficiency during standby load.
18. Further improvement of standby efficiency is realized by the built-in fss input correction function during burst (DC input detection mode). ***NEW***
19. Equipped with immediate latch stop function (SST terminal) by external signal.
20. Equipped with Vc1 OVP function (immediate latch stop)
21. 500KHz operation is possible by introducing control suitable for higher frequency.

1.2 Block Diagram

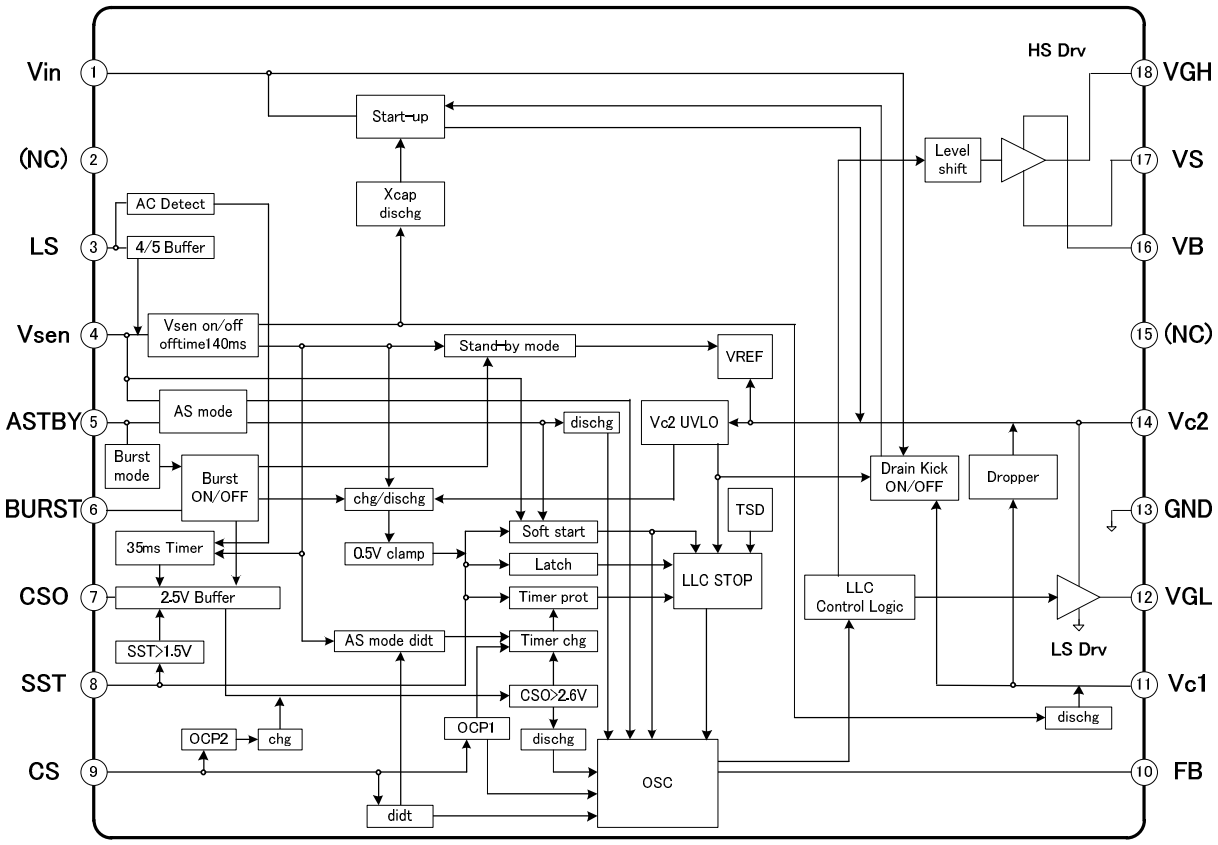


Fig 1 . MCZ5216ST Block Diagram

1.3 Pin Assignment

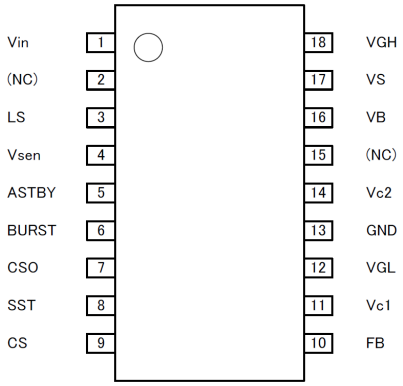


Fig 2 . MCZ5216ST Pin Assignment

1.4 Functions for each Pin

Pin No.	Symbol	Function
1	Vin	**Startup Circuit Input terminal, X-Cap Discharge terminal** This is the input terminal for start circuit, and equipped with X capacitor discharge function
2	(NC)	**Non-Connection Terminal**
3	LS	**AC Observation, Vsen Voltage Supply terminal.** Judgement of Input detection mode and voltage supply to Vsen terminal are performed by monitoring AC input.
4	Vsen	**Input Voltage Detection terminal. Low Input Protection, SS Reset** Low input voltage protection, remote ON/OFF, and SS reset are performed.
5	ASTBY	**Active Standby Switch terminal, Bust Mode Switch terminal** Active standby mode and burst mode are switched by external signal.
6	BURST	**Busrt Operation Control terminal** This is the terminal that control burst operation in burst mode.
7	CSO	**Overcurrent average detection response adjustment terminal, AC monitoring output terminal.** Adjusted the response when OCP 2 being detected and it is also power good signal output.
8	SST	**Terminals for Soft start, and for capacitor connection for intermittent operation during abnormal detection.** Determined the soft start time and the intermittent operation time during OCP1/2 operation.
9	CS	**Overcurrent detection, overcurrent averaging detection, di/dt (out of resonance) detection terminal.** Overcurrent(OCP1), Overcurrent average (OCP2), and di/dt detection terminals in LLC section.
10	FB	**Oscillator frequency setting terminal: Duty and operating frequency control** Set output feedback, various oscillation frequency (fmin, fmax, fss), and dead-time.
11	Vc1	**Vc2 Power Supply terminal** Perform Power Supply to Vc2 terminal.
12	VGL	**Low Side Driver Output terminal** This terminal is for Low side gate drive.
13	GND	**GND terminal** This terminal is for GND connection of IC's.
14	Vc2	**Control Circuit, Power Supply Output terminal for Driver** This terminal is for power supply output for gate drive.
15	(NC)	**Non-Connected terminal**
16	VB	**High-Side Driver Power Supply terminal** Power supply output terminal for high side gate drive.
17	VS	**High-Side Driver Reference Power Supply terminal** Connect to the source of high side MOSFET and the drain of the low side MOSFET.
18	VGH	**High-Side Driver Output terminal** High side gate drive terminal.

2 Discription of Basic Operation

※ See the characteristic diagrams in the characteristic specifications for the details of the characteristic diagrams stated in the Application Note. Unless otherwise specified, thresholds of MCZ5216ST are indicated by TYP values in the characteristic specifications.

2.1 Control Method of Each Operation

This section describes each operation mode of MCZ5216ST. Unless an operation mode is specified in the explanations from Sec 2.1 onwards, the following operation mode is used as a reference.

Input Voltage Detection Mode	AC Input Voltage Detection Mode
Oscillator Control Method	Symmetric Control
Operation Mode	Normal Mode

2.1.1 Input Voltage Detection Mode

MCZ5216ST has 2 input voltage detection modes.
Fig. 3 shows each connection method, and Fig. 4 shows each function in each detection mode.

For the following description onwards, each input voltage detection mode mentioned may be abbreviated.

x) AC Input Voltage Detection Mode ・・・ (Abbreviation) AC mode
y) DC Input Voltage Detection Mode ・・・ (Abbreviation) DC mode

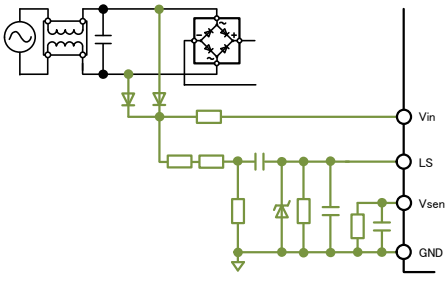
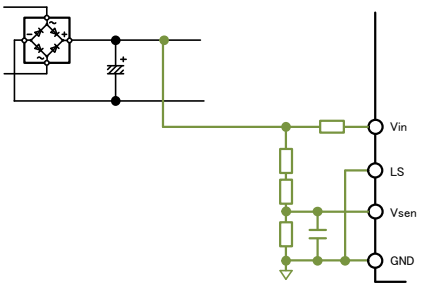
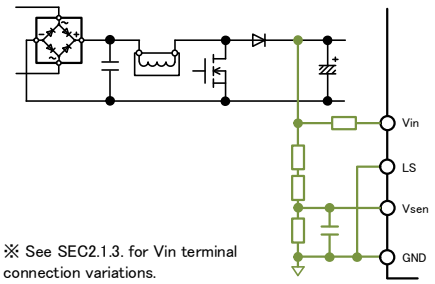
Input voltage detection mode	x) AC input voltage detection mode	y) DC input voltage detection mode
Assued connection condition	X-Capacitor discharge Function: Use	X-Capacitor discharge Function: Non-Use
connection point	Put before AC Bridge Diode	Put behind AC Bridge Diode OR behind PFC output Diode
connection diagram		  ※ See SEC2.1.3. for Vin terminal connection variations.

Fig 3. Connection Method of Input Voltage Detection Mode

Input voltage detection mode	x) AC Input voltage detection mode	y) DC Input voltage detection mode
Vsen ON/OFF threshold	Normal mode : 1.0V / 0.9V AS and Burst mode : 1.0V / 0.9V	Normal mode : 3.5V / 3.2V AS and Burst mode : 1.0V / 0.9V
X capacitor discharge function	Valid	Invalid
OCP input voltage correction	Valid	Valid (Varies according to Vsen voltage)
fss input voltage correction	Invalid	Valid
CSO Discharge Start/Delay time	35ms	0ms
SST Discharge Start/Delay time	140ms	0ms

Fig 4. Each Function of Input Voltage Detection Mode

2.1.2 Oscillator Control Method/ Operating Mode

MCZ5216ST has 2 control methods and 3 oscillator operation modes. Fig.5 shows the operating waveforms in each oscillator control and operating mode method.

【Oscillator Control Method】

a) Symmetric Control	High-side and low-side ON width ratio: Operation mode with 1:1
b) Asymmetric Control	High-side and low-side ON width ratio: Operation mode with 1:2

【Oscillator Operating Mode】

1) Normal Mode	Operation mode at rated load: This mode is set other than modes of 2) and 3). Assumed of a rated load such as load by 100%
2) Active Standby Mode (Called as in AS Mode)	Operation mode such as network standby at active standby operation. Assumed a load larger than standby such as 5% to 20% load.
3) Burst Mode	Operation mode at standby load. Assumed a load larger than standby such as 0 to 5%.

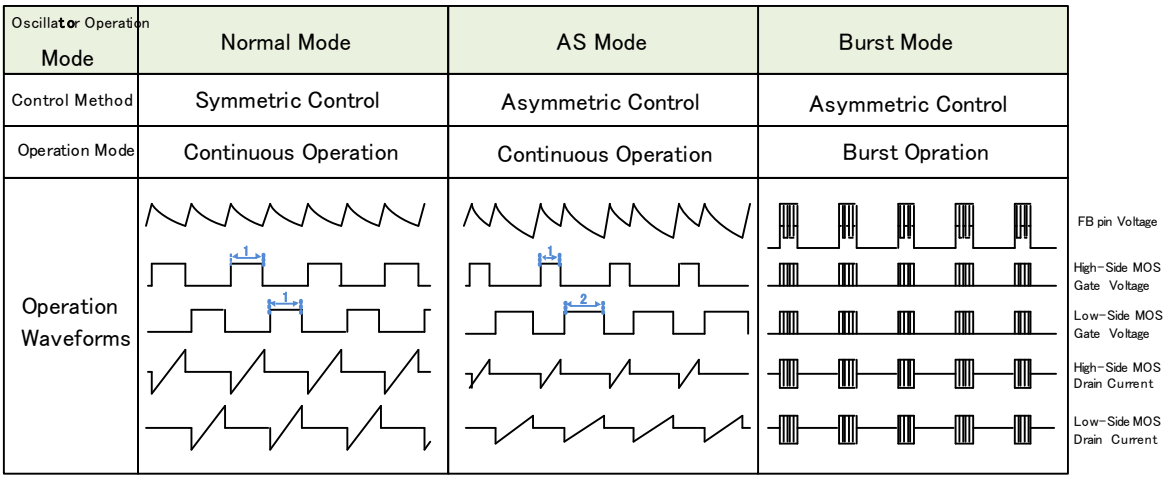


Fig 5. Operation waveforms in Various Oscillation Operation Mode

Each operation sequence of MCZ5216ST is shown in Sec 2.2 to 2.4.
See Sec 3 about constants determination method for each component.

2.1.3 HV startup

MCZ5216ST has a startup circuit that does not require a startup resistor. Its schematic diagram is shown in Fig 6, the connection methos is shown in Fig 7, and the sequences diagram is shown in Fig 8.

The Vin terminal is consisted by high-voltage switch, which charges C134 capacitor connected from high voltage section to Vc2 terminal, when the power is turned on.

After the power is turned on, a voltage is generated in the auxiliary winding Nc, and is applied to the Vc1 terminal via diode D161.The voltage generated in Vc1 terminal supply the voltage to Vc2 terminal due to internal dropper.

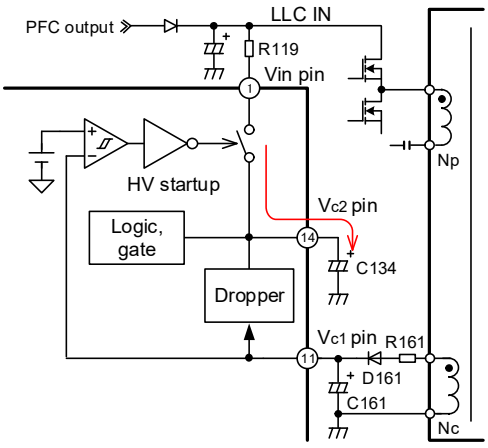


Fig 6. Schmatic Diagram of Self-Start Circuit

The supply current changes due to Vc2 terminal voltage to capacitor C134 connected from Vin terminal to Vc2 terminal. When Vc2=1V: Idk(on)1=2.8m A and when Vc2=4V: Idk(on)2=33.0m A.

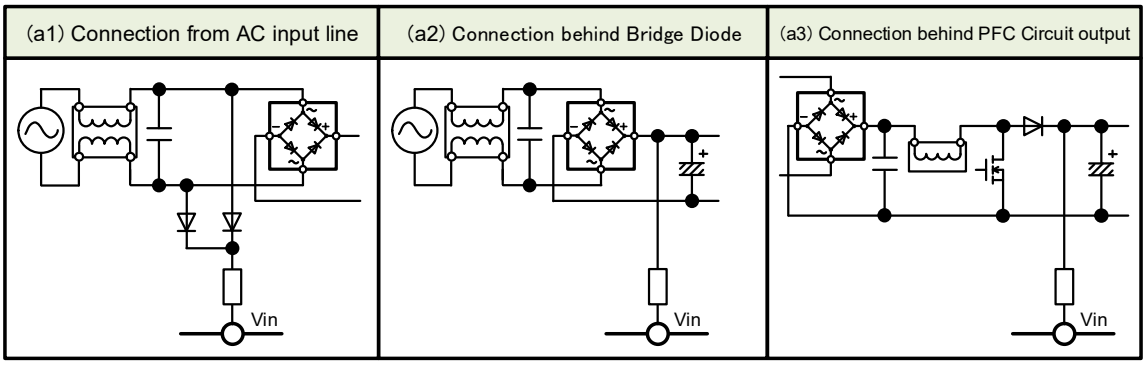


Fig 7. Connection method of Vin terminal

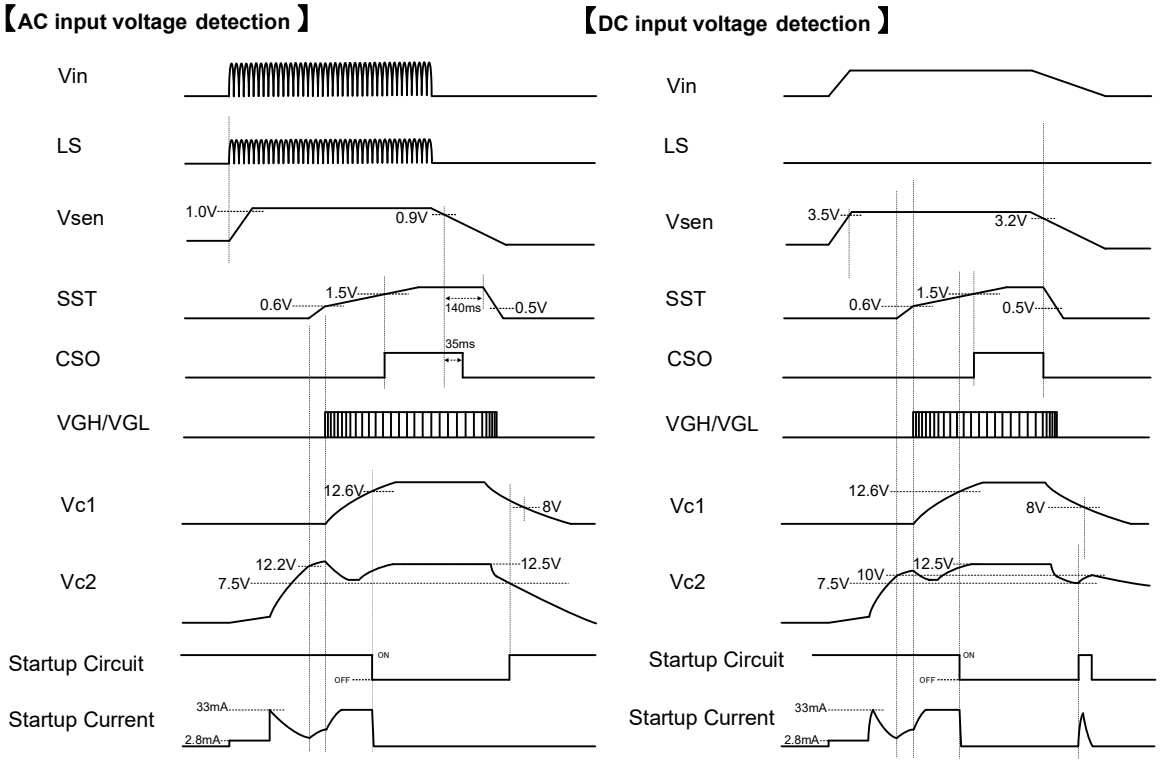


Fig 8. Startup Sequence in Various Detection Mode

【Vin Limitting Resistance R119】

Insert R119 shown in Fig 6, in case it is assumed that the abnormal condition short-circuited due to the contact the terminals for Vin and other low voltage between LLC In section and Vin terminal.

R119 needs to be designed so that the voltage applied to the Vin pin at the desired input voltage to start up tries not to fall below the recommended operating condition MIN(50V) (See Fig 9).

R119 is used with such as a fuse resistance and the resistance value is recommended in Table 1 below due to connection method in the Fig 7. Finally, please confirm with such as an abnormal test.

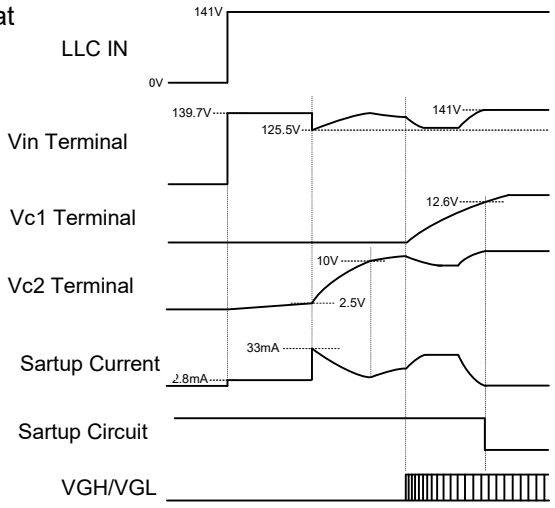


Fig 9. Startup example at R119=470ohm

Table 1. Recommended Resistance Value(R119)

Connect Method	Input Condition	Recommended Resistance Value
(a1)	AC100V system	100~470ohm
	AC200V system	1k~2.2kohm
	W/W system	100~470ohm
(a2)	AC100V system	100~470ohm
	AC200V system	1k~2.2kohm
	W/W system	100~470ohm
(a3)	PFC Boost 400V	1k~2.2kohm

【Vcc Limitting Resistance R161】

Insert a limiting resistor R161 to control short-circuit current between the auxiliary winding Nc and Vc1, when the power supply is started. R161 is recommended by approx.1 to 47ohm if the capacitors' value is 100 to 220uF, depending on capacitor's C161 capacitance.

In addition, it is recommended that the surge-resistance and pulse-resgistance are used as the current for charging C161 flows instantaneously when the power is turned on.

And if the R161 resistance value is increased, short-circuit current is suppressed at power supply startup, but it takes time until C161 voltage increases at the time of startup and burst mode, therefore, adjust resitance value of R161, after checking the time of startup and burst operation.

Table 2. Power Supply Threshold *Check details of each STD value in the characteristic specification document.

Item	Simbol	Condition	STD value	
Drain Kick Supply Current 1	Idk(on)1	Vin=100V、Vc2=1.0V	2.8	mA
Drain Kick Supply Current 2	Idk(on)2	Vin=100V、Vc2=4.0V	33	mA
Drain Kick Supply Current 1 & 2 Switching Vc2 voltage	Vc2(dkon12)	Idk=Idk(on)1→ Idk(on)2	2.5	V
Vc2 voltage at drain kick ON	Vc2(dkon)	Vin=100V、Vc1=0V	13.6	V
Vc2 voltage 1 at drain kick OFF	Vc2(dkoff)1	Vc1=16V、Vsen=6V、BURST<Vbst(H/L)	13.3	V
Vc2 voltage 2 at drain kick OFF	Vc2(dkoff)2	Vc1=16V、Vsen=6V、BURST>Vbst(H/L)	12.5	V
Drain kick stop Vc1 voltage	Vc1(dkoff)	Vin=100V	12.6	V
Drain kick restart Vc1 voltage	Vc1(dkon)	Vin=100V	8.0	V
Vc2 operation start voltage 1 (AC input detection mode)	Vc2(st)1	LS>Vls(acon)	12.2	V
Vc2 operation start voltage 2 (DC input detection mode)	Vc2(st)2	LS<Vls(acon)	10.0	V
Vc2 operation stop voltage	Vc2(sp)		7.5	V

2.2 AC description of input voltage detection mode operation

This Section shows the operation of AC input voltage detection mode.

2.2.1 Power supply (AC input voltage detection mode)

The sequence of power startup operation in the AC input voltage detection mode is shown in Fig 10.

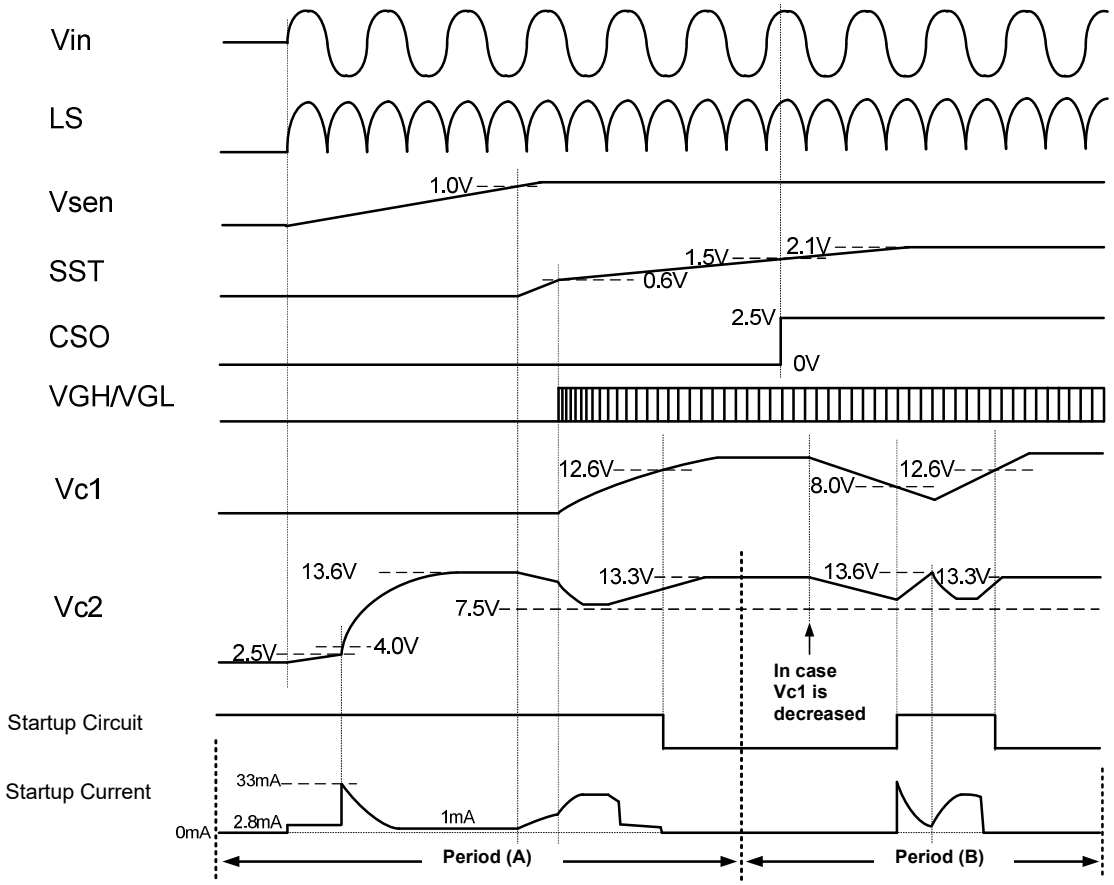


Fig 10. Startup sequence Diagram at AC input voltage detection mode

【Period (A)】

When power is turned on, if Vc1(dkoff) terminal voltage is less than 12.6V, Vc2 terminal voltage is charged until it rises to 13.6V. When Vc2 terminal voltage increases by 12.2 or more and Vsen terminal voltage rises to 1.0V or more, charging of SST terminal starts. And when the voltage of SST terminal voltage (Vss(st)) becomes 0.6V, the power supply operation starts as the LLC gate is ouput.

When the power supply operates and a voltage is generated in the auxiliary winding Nc, the capacitor C161 is charged and Vc1 terminal rises. When Vc1 terminal voltage exceeds Vc1(dkoff) of 12.6V, the starter circuit is disconnected and only supply from the auxiliary winding. In that case, the maximum value of the Vc2 terminal voltage in clamped to Vc2(dkoff)1 of 13.3V.

【Period (B)】

When the Vc1 terminal voltage drops to Vc1 (dkon) of 8.0V or less, the start circuit operates again. When the Vc2 terminal voltage drops to Vc2 (sp) of 7.5V, MCZ5216ST stops.

Insert capacitors that can operate stably in transient states such as startup and disconnection for the capacitors (C134 and C161) connected to terminals of Vc1 and Vc2. It depends on the desired input/output conditions, but the capacitors (47u to 470uF) are recommended.

In addition, if the position of C134 and C161 is far from Vc1 or Vc2 of MCZ5216ST, a malfunction may be occurred because noise may be entered. In this case insert MLCC of approx. 0.1u to 1.0uF near the Vc1 and Vc2 terminals to prevent malfunction.

The AC input voltage detection mode assumes Vc1 and Vc2 power supply using a self-starting circuit, therefore, external Vcc startup, which starts by appliying the external power supply to Vc1 terminal without using the self-start circuit, cannot be performed. So when using the AC input voltage detection mode, start by connecting the self-start circuit due to the Vin terminal.

2.2.2 X Capacitor discharge / Input voltage detection function (LS, Vsen terminal)

When using the AC input voltage detection mode, X capacitor and power good signal(CSO terminal) are equipped. And after Vsen terminal voltage gets lower than Vsen2 (0.9V), CSO terminal becomes low after 35ms, and SST terminal discharge and X capacitor discharge function becomes ON after 140ms. The detailed sequence shows in Fig 11.

In the AC input voltage detection mode, it is assumed that the load gets light by transmitting the stop signal secondary side by becoming low of the power good signal(CSO terminal).

When not using the power good signal, Vsen terminal voltage repeats with Gate On/Off after Vsen becomes lower than theshold voltage(Vsen2) during 140ms, therefore, the input voltage of LLC section tends to lower easily. The frequency is limted by the OCP2 operation until 35ms passage after the voltage falls below threshold (Vsen2) value, but after passing 35ms, CSO gets low, therefore, the overcurrent protection function becomes only OCP1 or di/dt protection function.
For the above reason, the protection for OCP1 and di/dt protection may continue operating during 140ms.

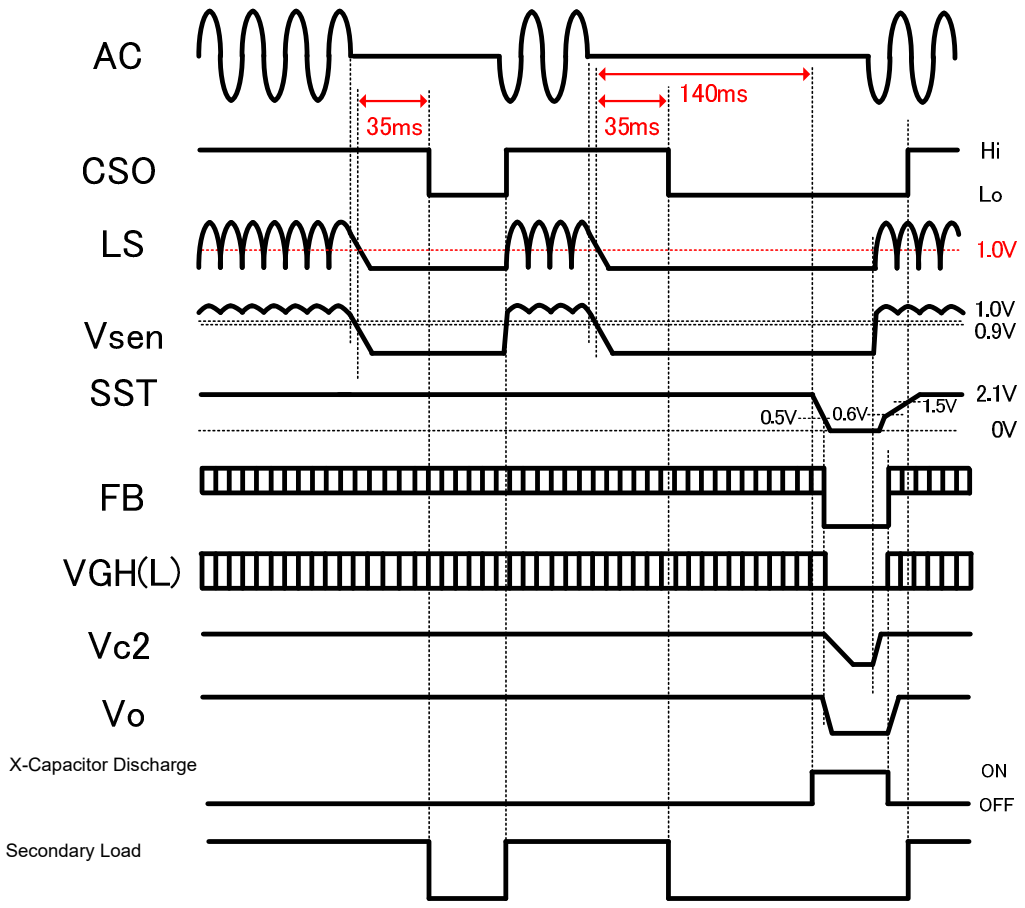


Fig 11. X Capacitor discharge function operation sequence

2.3 DC Input voltage detection mode operating

This section shows the operation in DC input voltage detection mode.

2.3.1 Power supply (DC input voltage detection mode)

Fig 12 shows the operation sequence at power-on in DC input voltage detection mode.

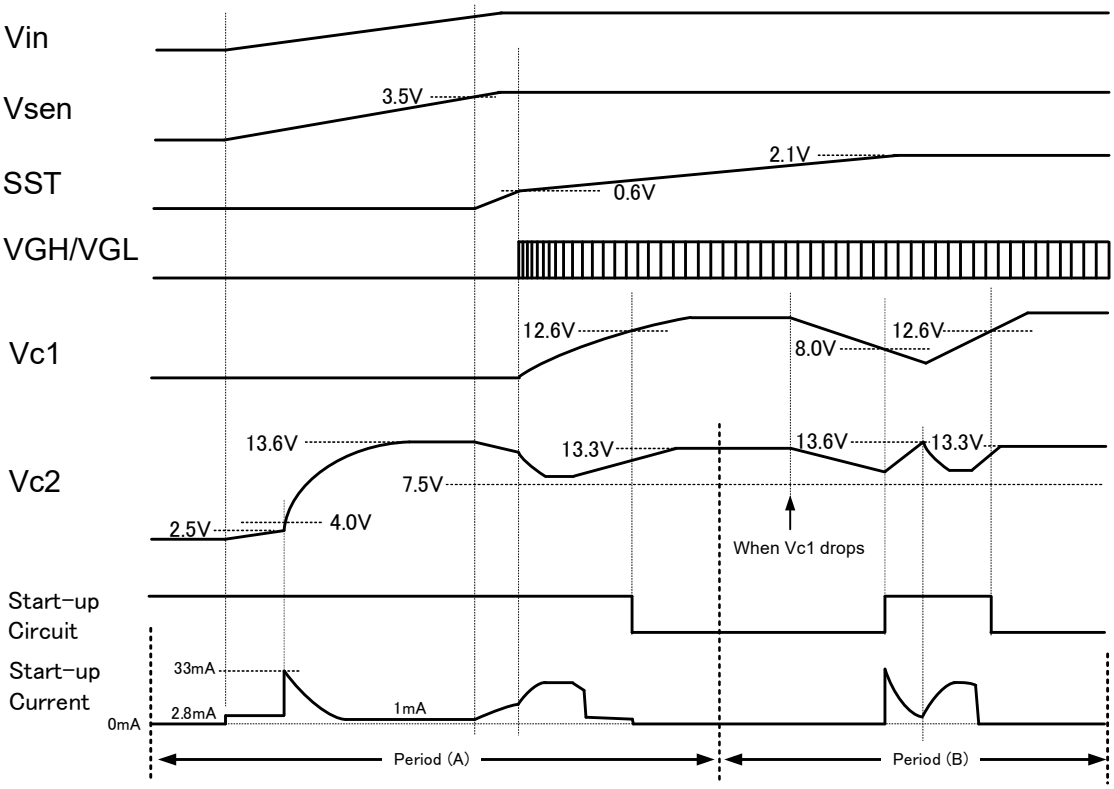


Fig 12. Startup sequence at DC input voltage detection mode

【Period (A)】

When the power is turned on, if the Vc1 terminal voltage is less than Vc1(dkoff) 12.6V, the Vc2 terminal voltage is charged until the voltage becomes 13.6V. And if Vc2 terminal voltage increases by 10.0V or more, and if Vsen terminal voltage gets to 3.5V or more, the charge to SST terminal starts, and as soon as SST terminal voltage gets to Vss(st) 0.6V, the LLC gate is output and power supply operation starts.

When the power supply operates and a voltage is generated in the auxiliary winding Nc, the capacitor (C161) is charged and Vc1 terminal voltage rises. When the Vc1 terminal voltage exceeds Vc1 (dkoff) 12.6V, the starter circuit is only supplied from the auxiliary winding by the starter circuit being disconnected. In this case, Vc2 terminal voltage is clamped by Vc2(dkoff)1 13.3V

【Period (B)】

Vc1 terminal voltage become lower until Vc1(dkon) 8.0V, the startup circuit operates again. When Vc2 terminal voltage decrease til Vc2(sp) 7.5V, MCZ5216ST stops.

For the capacitors (C134 and C161) connected to Vc1 terminal and Vc2 terminal, insert capacitors that can operate stably in transient states such as start-up and disconnection. It depends on the desired input condition, 47u to 470uF is recommended.

In addition, if the external Vcc by DC input voltage detection mode without using the self-start circuit is started, it may be able to make the capacitance of capacitor (C134 and C161) small. If the voltage applied to Vc1 terminal is stable, it is recommended that capacitor C134 be around 4.7u to 47uF and C161 be about 10 to 100uF.

If capacitors (C134 and C161) location is far from the terminals of Vc1 or Vc2, a mulfanction may be occurred because noise may enter. In that case, insert MLCC of around 0.1u to 1.0uF near Vc1 terminal and Vc2 for preventing from mulfanction.

Fig 13 shows the sequence diagram at active standby ON/OFF during DC input voltage detection mode. The threshold value (Vsen) varies though the active standby mode operation sequence will be described in the later pages.

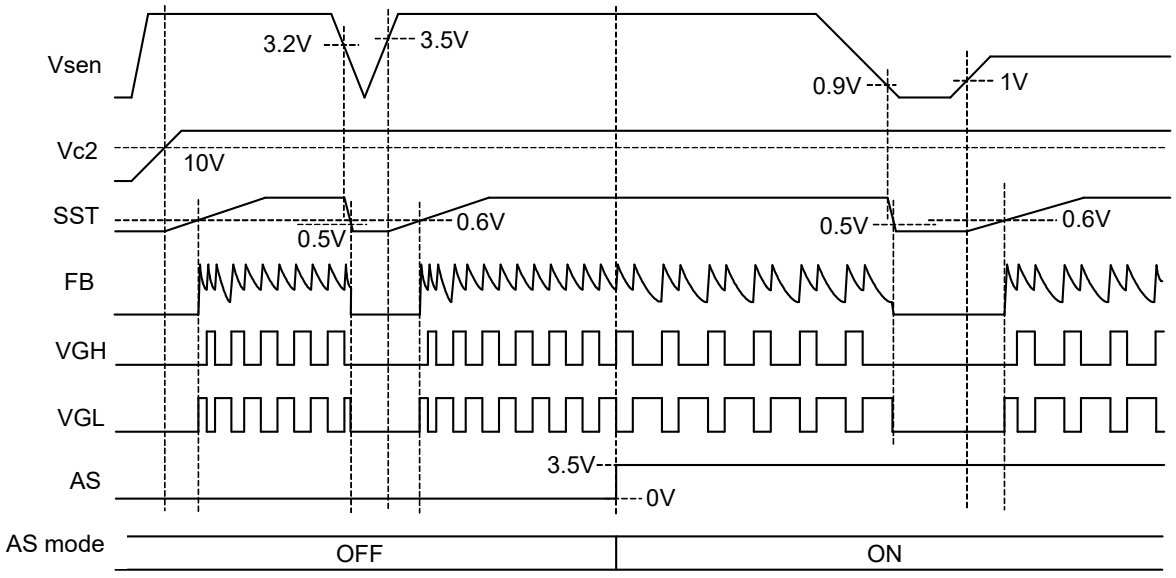


Fig 13 . Vsen terminal and each output timing chart (During AS OFF and AS ON operation)

2.4 Discription of Each mode common terminal operation

2.4.1 Gate driver output (VGL、VGH terminal)

The gate output is output from the terminals of VGL (low side MOSFET), and VGH(high side MOSFET). Plese see Sec. 2.4.2 for Gate output timing.

LLC gate driver drive capability is 0.24A(Source)/0.40A(Sink). This value is designed to drive the MOSFET fast enough without causing a signal malfunction.

Fig. 14(A) shows a drive circuit used generally.

Connect a diode for Sink as shown in Fig. 14(B), when using a MOSFET with a large Qg. When using a diode for Sink, use a small capacity Schottky Barrier Diode, etc., and do not use a snappy (hard) recovery diode. It is recommended that D1NS4(axial) and M1FM3(SMD) are used.

And if you want the switching speed to increase at turn-off, connect sink buffer circuit shown as Fig. 14(C)

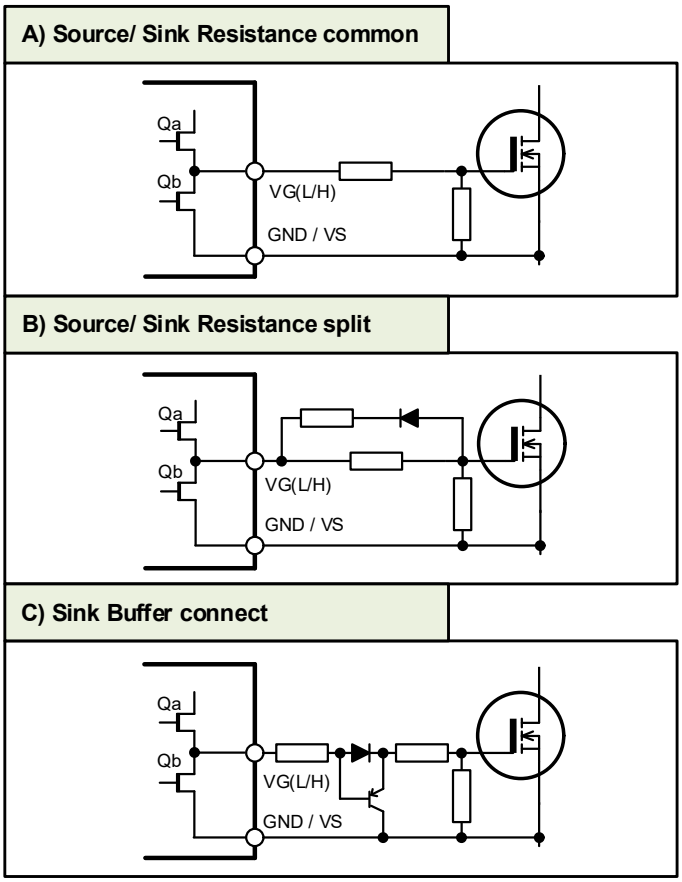


Fig 14 . Gate drive circuit example

Table 3. Drive capability threshold Value Check each detailed STD value in the characteristics Spec document.

ITEM	Simbol	Condition	STD Value	
Source drive capability	Iout(so)	VGL=VGH=0V	-240	mA
Sink drive capability	Iout(si)	VGL=VGH=12V	400	mA

2.4.2 Oscillation Control Section (FB terminal)

The oscillation frequency of MCZ5216ST is determined by charge/discharge of the capacitor (Ct) connected to the FB terminal. The FB terminal voltage and the ON/OFF timing of each gate output(VGL, VGH) is shown in Fig. 15.

When the FB terminal voltage falls below the Vfb(bottom) voltage, the Ct capacitor connected to the FB terminal is charged by Ifb(chg). When the FB terminal voltage exceeds above the Vfb(top) voltage, the charging is stopped by Ifb(chg) and the discharge of Ct capacitor is performed by the Rt and FB resistance connected to the FB terminal

While The FB terminal is discharging, VGL and VGH alternately turn on. In addition, while the FB terminal is charging, the dead time(DT) that VGL and VGH turn off simultaneously is come.

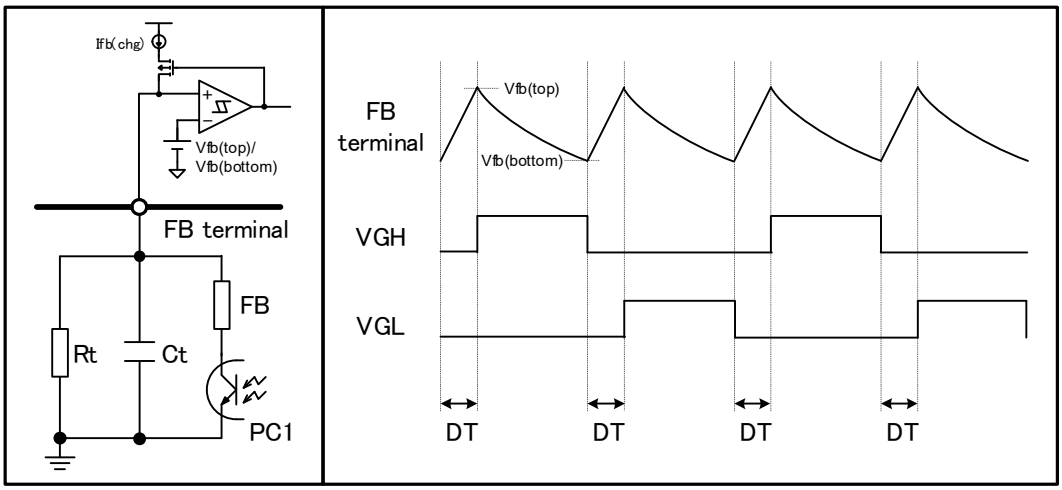


Fig 15 . FB terminal connect and VGH、VGL operation waveform

FB terminal charge/discharge timing for each operation mode is shown in Fig. 16

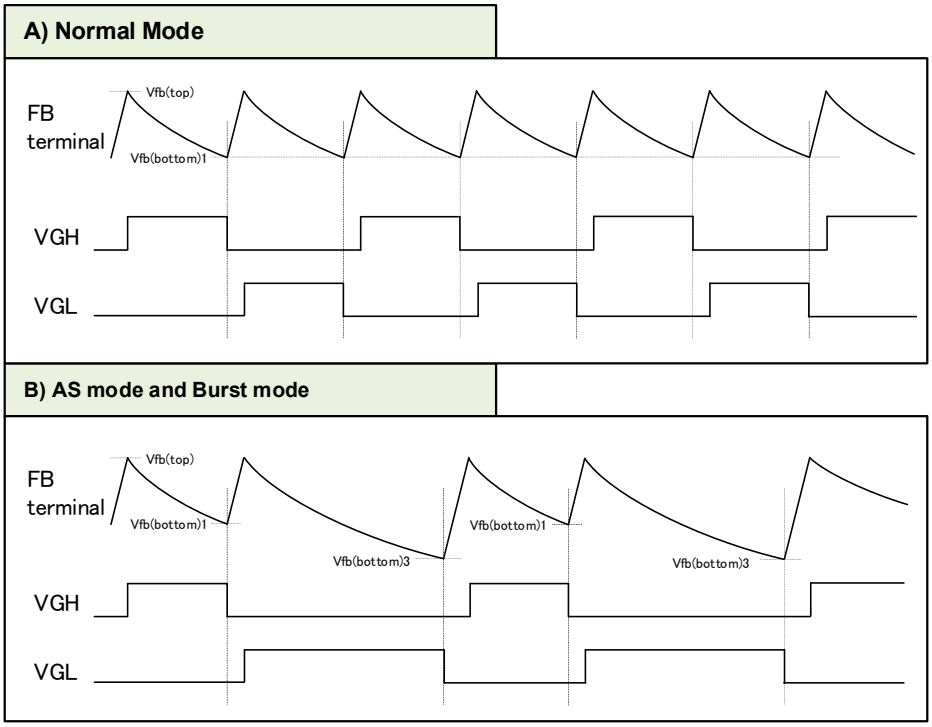


Fig. 16. Gate ON/OFF timing in each operation Mode

MCZ5216ST is a IC of the frequency and ON duty modulation. The oscillation frequency is controlled by the FB terminal current. The oscillation frequency gets higher by reducing the Rt resistance value (The current get larger flowing to the FB terminal) such as relationship between the Rt resistance value and oscillation frequency in Fig. 17.

Like the relationship between the oscillation frequency and the dead time in the Fig. 17, the dead time varies according to the oscillation frequency. Under the conditions where the oscillation frequency is maximized, during such as the light load, the dead time is controlled widely, therefore, it is easy for ZVS(Zero Voltage Switching) to ensure throughout the entire frequency range.

The minimum oscillation frequency (fmin) is determined by the external resistance of Rt connected in parallel with the capacitance of the Ct capacitor connected to the FB terminal.

The maximum oscillation frequency (fmax) is determined by the value of Rt and FB resistance connected in parallel with the Ct capacitor capacitance connected to the FB terminal.

During continuous operation, the maximum oscillation frequency (fmax) is recommended by lower than 500KHz.

And the initial oscillation frequency (fss) varies depending on the Ct capacitor capacitance at the soft start operation (See Sec 2.4.5).

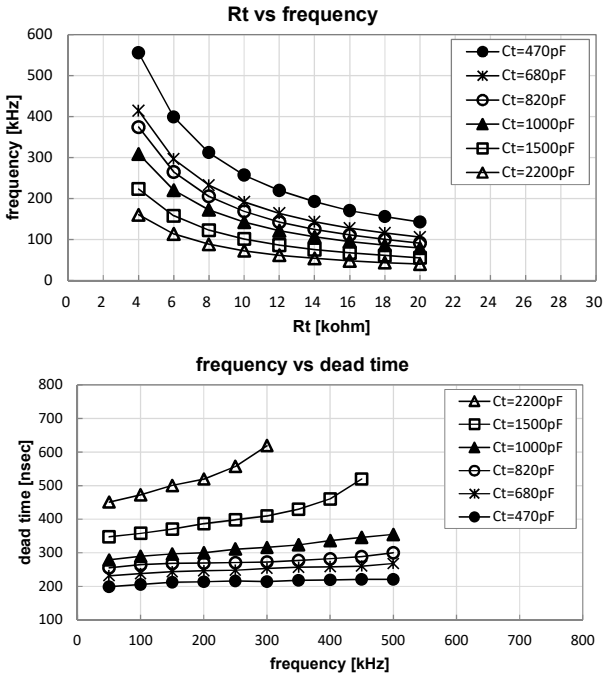


Fig 17. Relationship between Rt resistanc, Oscillation Frequency (Above) and between Oscillation Frequency and Dead time (below)

Table 4. FB terminal threshold valu. Check details of each STD value in characteristics spec.

Item	Simbol	Condition	STD value	
FB Charge Current	Ifb(chg)	FB=4V	-11.0	mA
FB Charge Stop voltage	Vfb(top)		5.00	V
FB Charge start voltage 1	Vfb(bottom)1		3.75	V
FB Charge start voltage 3	Vfb(bottom)3	ASTBY=open	2.80	V

2.4.3 Overcurrent Protection Function(CS, CSO terminal)

MCZ5216ST equip the overcurrent protection function, and the detection is perfomed by CS terminal. Fig. 18 shows a connection example of the CS and CSO terminals. In the following pages, the calculation formulars and etc when detecting with the resistance partial voltage in Fig. 18 (a) are shown.

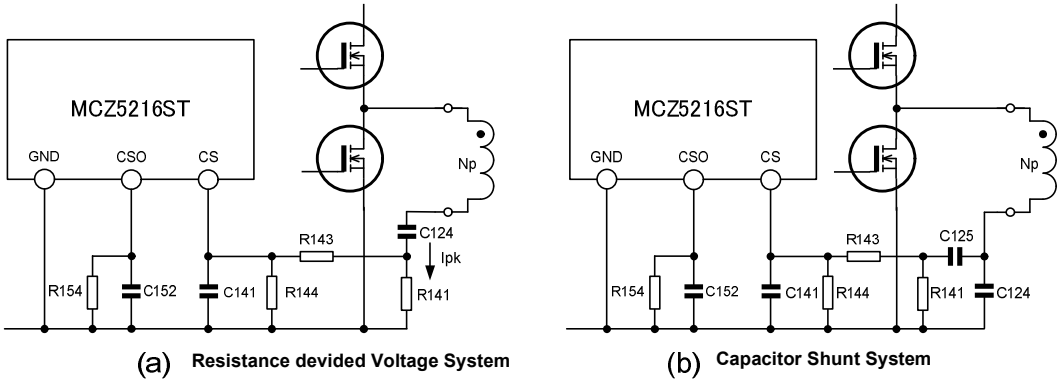


Fig 18. Connexion example of CS and CSO terminal

As shown in Fig. 18(a), the current flowing through the resonance capacitor C124 is detected by the current detection resistor R141,and connect to the CS terminal by dividing with divide resistance R143 and R144. See Sec 3.5 for calculation method of each resistance value.
In addition, C141 is a filter capacitor. When R143 is set to 10ohm, adjust approx. 0.01uF to the initial value.

The CS terminal has 3 threshold value each for both the positive and negative directions, the 3 kinds of protection function is operated depending on its voltage levels. Each protection function is defined as OCP1, OCP2 and di/dt here.

Table 5. Overcurrent Protection(3 Functions)

	Simbol	Discription	CS terminal Threshold Condition
①	OCP1	Cycle by cycle OCP	CS terminal voltage exceeds ±0.500V
②	OCP2	Frequency limit OLP	CS terminal voltage exceeds ±0.350V
③	di/dt	Capacitive mode protection	CS terminal voltage decreases ±0.060V

*OCP : Over current protection, OLP : Over load protection

【OCP1】

OCP1 starts operation when the CS terminal exceeds +/-0.500V. This is an OCP that assumes a load short circuit. Fig 19 shows example of OCP1 detection operating while the high-side MOSFET is on. During the high-side period, when the CS terminal voltage rises above +0.500V, the OCP1 detection operates. Similarly, during the low-side period as well, the CS terminal voltage falls below -0.500V, the OCP1 detection operates.

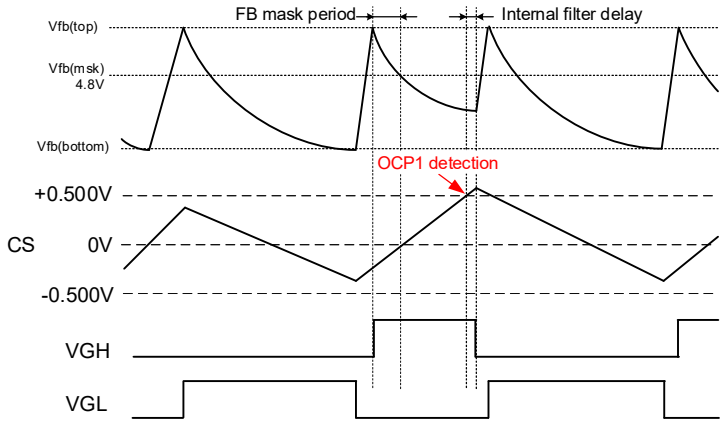


Fig 19. OCP1 Operation Sequence

When OCP1 detection is operated, MCZ5216ST performs the following control.
(a) the FB terminal switches to the charge period, and the gate output (VGL or VGH) turns off.
(b) Charge the SST terminal at 40uA for 8 cycles of FB charge/discharge.
When the FB terminal rises till Vfb(top), another side of the gate output (VGL or VGH) turns on.

The gate output turns off immediately when OCP1 is detected, therefore, during the abnormality, the current-peak flowing to the MOSFET is controlled, and overcurrent/transformer saturation are protected. Also, as shown in Sec. 2.4.5, the SST terminal is charged by timer and the oscillation operation is stopped and restarted, when the abnormal state continues for a long time. In case the abnormal state continues after even the restart, similary the charge is done by timer and the latch is stopped. Due to this, it enables MOSFET and the other components to prevent from abnormal heating

If OCP1 is not detected again within 8 cycles of FB charge/discharge after OCP1 is detected, the SST terminal becomes refresh operation and discharges SST terminal til become 2.1V with Timer discharge current (refresh) 80uA.

((FB Mask Period))

To prevent OCP1 detection malfunction due to a noise generated by switching when the MOSFET turns on and off, the CS terminal is masked so that the OCP1 tries not to operate until from starting the discharge of FB terminal through becoming FB mask voltage and below. Therefore, OCP1 operation is not performed even if the threshold is exceeded during this period. If the minimum oscillation frequency (fmin) of MCZ5216ST is designed too low, the OCP1 threshold value maybe exceeded and masked during the period longer than FB mask voltage, so please design an appropriate fmin.

((Internal Filter))

To prevent a malfunction due to a noise caused by external factors and etc., internal filter (approx. 300ns) is integrated. As a result, a delay of approx. 300ns is happened from when the CS terminal exceeds the OCP1 threshold til when FB starts charging.

((About detecting OCP1 and OCP2 simultaneously))

Since OCP1 and OCP2 are detected by the same terminal, the period reaching OCP1 detection threshold exceeds the OCP2 detection also threshold. In that case, the gate output is turned off immediately by OCP1 detection while charging CSO by OCP2.

【OCP2】

OCP2 operates when the CS terminal exceeds +/-0.350V.
When OCP2 operates, MCZ5216ST performs the following control.

(a) The SST terminal is charged for 8 cycles of FB charge/discharge. The charging current changes depending on the CSO terminal voltage.

- 2.5V≦CSO＜2.6V : The charging to the SST termnal does not perform.
- 2.6V≦CSO＜3.6V : The SST terminal is charged at 1.7uA.
- 3.6V≦CSO≦4.0V : The SST terminal is charged at 40uA.

(b) The CSO terminal is charged at 20uA for the period up to the FB mask voltage in the next cycle of OCP2 detection.

Like OCP1, the OCP2 has an FB mask period and an internal filter as well. If the fmin is designed too low, the OCP2 threshold may be masked by exceeding during the period longer than the FB mask voltage, please design an appropriate fmin.

If OCP2 is not detected within 8 cycles of FB after OCP2 is detected, the SST terminal discharges the SST terminal with Timer discharge current (refresh) 80uA until it reaches 2.1V.

【CSO】

The CSO terminal controlls the oscillation frequency according to the CSO terminal voltage. Fig 20. shows relationship between the CSO terminal voltage and the oscillation frequency. The CSO terminal is pre-charged inside of the IC and is usually maintained at 2.5V.

When the aforementioned OCP1 and OCP2 operate, as Fig 21. shows, the CSO terminal is charged and when the CSO terminal voltage exceeds 2.6V, the oscillation frequency increases according to the CSO terminal voltage. The output power is limited by increasing the oscillation frequency. The CSO terminal is charged up to 4.0V at max.

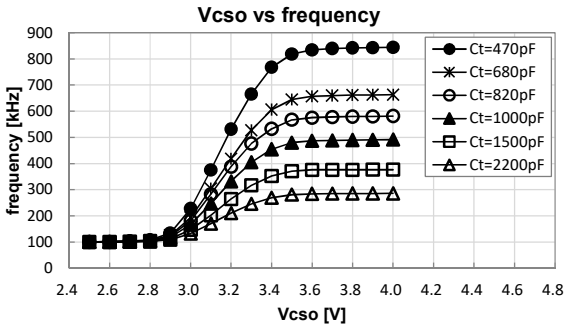


Fig 20. CSO Voltage VS Oscillation Frequency

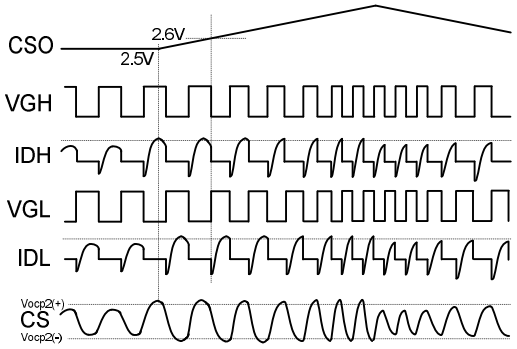


Fig 21. CSO Voltage Operation Sequence

【di/dt】

di/dt operates by detecting the negative edge where the CS terminal falls below +/-0.06V as shown in Fig 22. When di/dt operates, MCZ5216ST performs the following control.

(a) The FB terminal switches during the charging period and turns off the gate output(VGH or VGL).

(b) The SST terminal is charged according to the operation mode.

- Normal Mode : Charging to the SST terminal is not perfomed.
- Active Standby Mode : The SST terminal is charged at 40uA for 8 cycles of FB charge/discharge.
- Burst Mode : The SST terminal is charged at 40uA for 8 cycles of FB charge/discharge.

When di/dt operation is performed, the gate output is turned off immediately, therefore, it enables loss of resonance(Capacitive mode) to be prevented from abnormal heating and damage of the MOSFET.

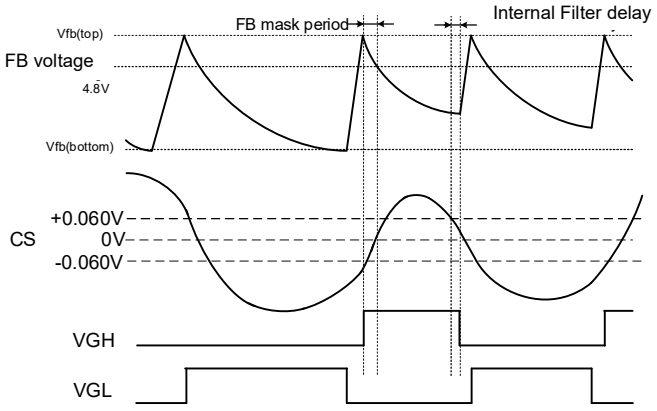


Fig 22. di/dt Operation Sequence

di/dt has the FB mask period and the internal filter as well as OCP1 and OCP2
If fmin is designed too low, it may be masked while trying to detect the di/dt threshold during the period longer than the FB mask voltage. Design an appropriate fmin.

Table 6 shows the relationship between Timer and CSO charging in each detection mode.

Table 6. Timer and CSO charging operation relation table in each detection mode

Detection Mode	Operation Mode	Timer Charging	CSO Charging
OCP1Detection	Normal Mode	(A)	(B)*1
	Active Standby Mode		
	Burst Mode		
OCP2 Detection	Normal Mode	(C)	(B)
	Active Standby Mode		
	Burst Mode		
di/dt Detection	Normal Mode	None	None
	Active Standby Mode	(A)	
	Burst Mode		

(A) Charge the SST terminal at 40uA for 8 cycles of FB.

(B) Charge the CSO terminal at 20uA for the period up to FB mask voltage in the next cycle of OCP2 detection. *1 By OCP2 detection, CSO is charged

(C) The SST termminal is charged at 1.7uA(2.6V≦Vcso<3.6V), and 40uA(3.6V≦Vcso≦4.0V) for 8 cycles of FB.

Table 7. CS・CSO terminal threshold value. Check detail for each STD value in characteristics spec.

Item	simbol	Condition	Standard	
OCP1(+) Detection Voltage	Vocp1(+)		0.500	V
OCP1(-) Detection Voltage	Vocp1(-)		-0.500	V
OCP2(+) Detection Voltage 1	Vocp2(+)1		0.350	V
OCP2(-) Detection Voltage	Vocp2(-)		-0.350	V
di/di(+) Detection Voltage	Vdidt(+)		0.060	V
di/dt(-) Detection Voltage	Vdidt(-)		-0.060	V
CSO terminal Precharge Voltage	Vcso(pre)	CS=0V	2.5	V
OCP2 operation start CSO terminal voltage	Vcso(ocp2)		2.6	V
Timer charge switch CSO terminal detection voltage	Vcso(tmr)		3.6	V
During OCP2 operation CSO terminal charge current	Icso(ocp2)	CSO>Vcso(ocp2)	-20	uA
CSO terminal discharge current	Icso(dis)	CSO=2.8V	10	uA

2.4.4 OCP2 input voltage correction (CS Terminal)

MCZ5216ST has a buit-in circuit to correct the overcurrent protection operating point when the input voltage fluctuates. Input voltage correction is performed by changing detection threshold value of the OCP2. The threshold value of the OCP2 varies according to the FB terminal voltage.

Fig 23. shows a schematic diagram of the drooping characteristics with and without the input correction function. Especially, when high input voltage is applied, correction for OCP2 detection is easily performed.

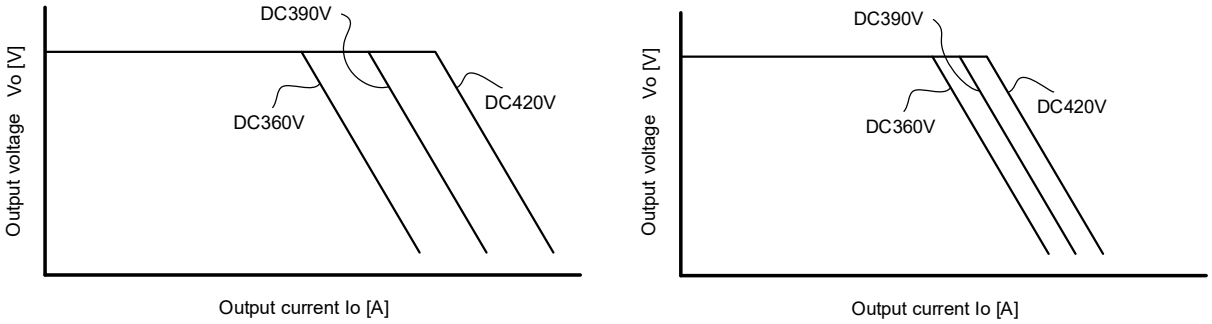


Fig 23. OCP2 Schematic diagram of drooping characteristics without input correction function(left) and with correction function (right)

Fig 24. shows resonance curve and operation waveform of the LLC current resonance circuit. As shown in the operation waveform of Fig 24.(a), the oscillation frequency changes depending on the input voltage during operation changes. Generally, for the same load, the lower the input voltage is applied, the higher the peak of the current waveform gets. The resonance frequency(fr) is constant regardless of the input voltage.

Assuming that the overcurrent protection function works at the point where the MOSFET current value reaches the peak value (points X and Y) as shown in Fig 24(b), the MOSFET current value changes, depending on the input voltage where it reaches the peak while the gate turns on. For example, shown in Fig 24(b), if the period is as 1 during the gate turn-on, the cuurent peaks is come during the on-period with a duty ratio of 0.8:0.2 when the input voltage is high. On the other hand, if the input voltage is low, the cuurent peak is come during on-period with a duty ratio of 0.4:0.6

In this way, if the gate is on when the input voltage is low, the current peak comes before the on-period (point Y). When the input voltage is high, it comes later in the on period (point X). The input voltage of OCP2 is corrected using this resonance characteristic.

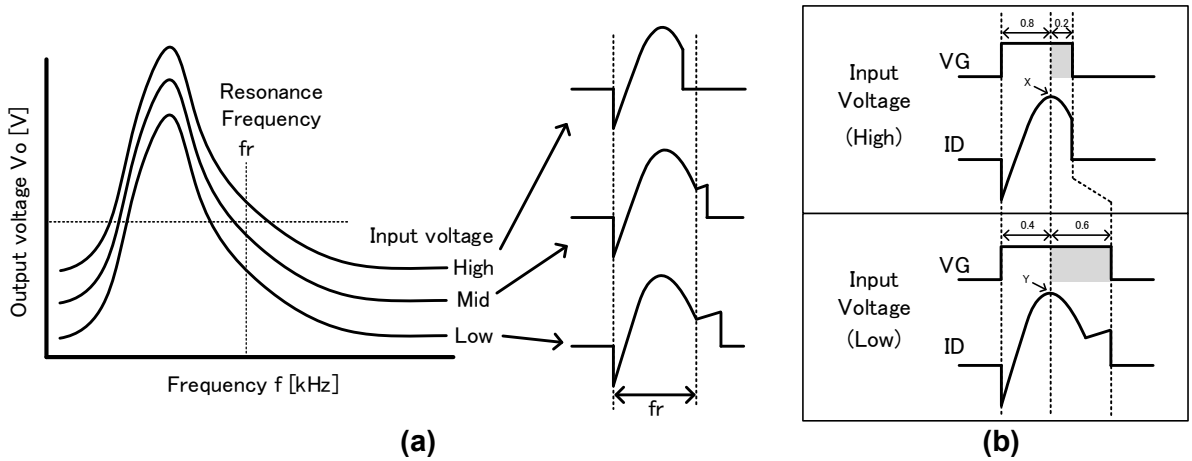


Fig 24. (a) input voltage and operation waveform, (b) input voltage and current peak

Input correction is adjusted by changing the OCP2 detection threshold so that OCP2 can be detected easily.

Fig 25(b) shows threshold value (Vocp2(+)) when the FB terminal voltage changes. As shown in Fig 25(b), the OCP2 detection threshold value(Vocp2(+)) is 0.35V after the FB terminal ends the FB mask period. The lower the FB terminal goes gradually, the lower the threshold value of Vocp2(+) falls, and the Vocp2(+) is 0.25V in the FB charging start voltage(Vfb(bottom)).

The input correction circuit is included only in the high side period.
During the low side period, the threshold is always -0.35V regardless of the FB terminal voltage.

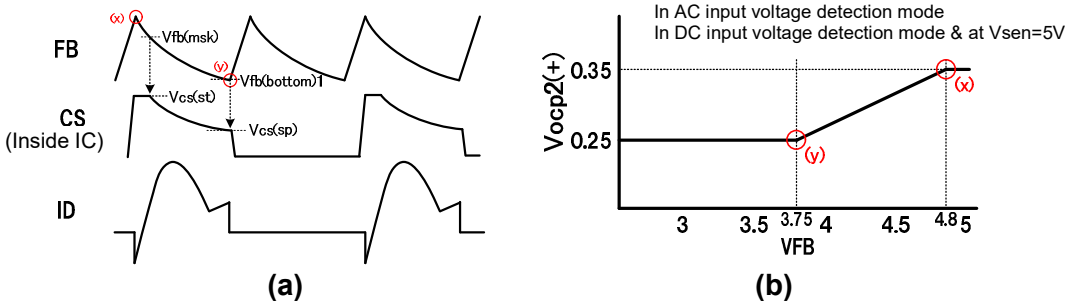


Fig 25. (a) CS internal Operation wafeform, (b) FB Voltage･CS internal threshold value

This correction level changes in AC input voltage detection mode and DC input voltage detection mode.

【During AC input voltage detection mode 】
Vcs(sp) is LS terminal, which is +0.25V regardless of the Vsen terminal voltage.

【During DC input voltage detection mode 】
Vcs(sp) changes depending on Vsen terminal voltage.
When Vsen=4.5V, Vcs(sp)=+0.25V, and when Vsen=3.2V, Vcs(sp)=+0.35V.

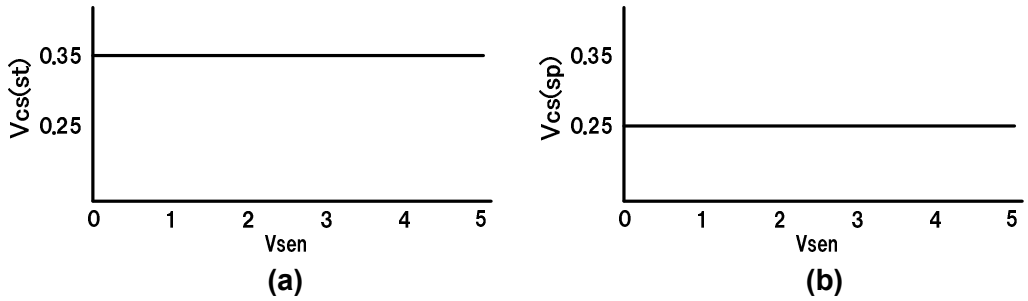


Fig 26. During AC input voltage detection mode, (a) Vcs(st):threshold value, (b) Vcs(sp):threshold value

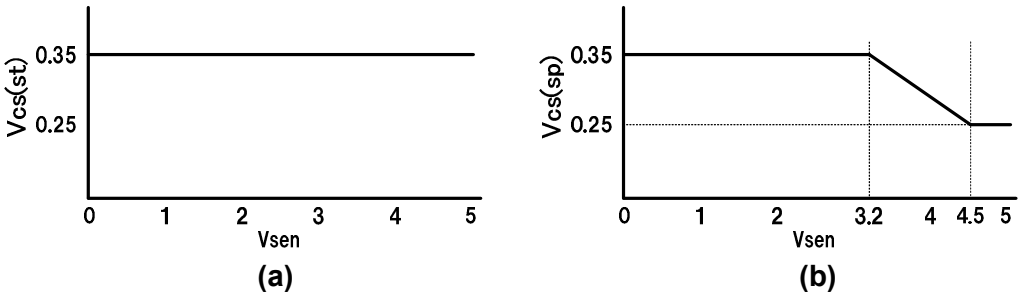


Fig 27. During DC input voltage detection mode, (a) Vcs(st):threshold value, (b) Vcs(sp):threshold value

2.4.5 Soft Start, during startup di/dt protection, Latch stop function (SST Terminal)

(1) Soft Start function

MCZ5216ST has a built-in soft start function, the oscillation frequency increases gradually by charging the capacitor connected to between SST terminal and GND. The following two condictions must be satisfied for the SST terminal to be charged.

① Vc2 terminal voltage is higher than the Vc2 operation start voltage.
・AC input voltage detection mode: 12.2V, DC input voltage detection mode: 10.0V

② Vsen terminal voltage is equal or higher than the input voltage monitoring voltage threshold.
・AC input voltage detection mode: Vsen1 or Vsen3, DC input voltage detection mode: Vsen5 or Vsen7

Oscillation starts at SST terminal 0.6V or more, and becomes constant at Vsst(open) 2.1V. And also, it has hysteresis and stops oscillation at SST terminal 0.5V or less. See Fig 28. for the relationship between SST terminal voltage and oscillation frequency.

SS charge current of the SST terminal is 2 stages according to the SST terminal voltage. If the SST terminal voltage is from 0V to 0.6V, it charges at 90uA. And if the SST terminal voltage is 0.6V or more, it charges at 30uA. This is switched to speed up the charging to the LLC operation start SST voltage.

The SST terminal is charged to 2.1V and is clamped at that voltage during normal operation.

In addition, the SST terminal has a timer intermittent latch stop function to reduce the load on the main switch and peripheral circuits during abnormal situation. See Sec 2.4.5(3) on the detail of the timer intermittent latch stop function.

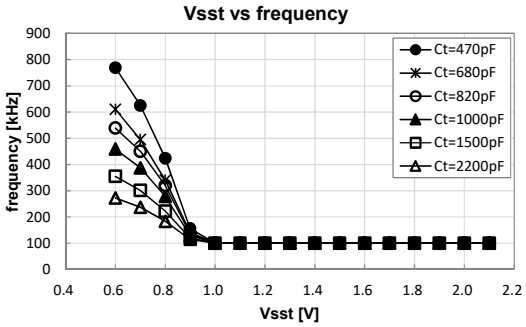


Fig 28. SSTvoltage & oscillation frequency

(2) During startup di/dt protection

Immediately after the power supply operation of the LLC current resonance circuit starts, in the transient state where the voltage of the resonance capacitor is unstable, the gate may turn off while the current flowing through the MOSFET flows through the body diode. In this state, a short-circuit current flows when the opposite MOSFET turns on due to the trr composition, and a load is applied to the MOSFET. MCZ5216ST has a built-in Tss(3) function to prevent the gate from turning off while the body diode is conducting at startup.

As shown in Fig 29, Tss(3) sequence extends the low-side VGL output for the second time by 1.7 times, after the power supply operation starts. This allows the gate output to be turned off after the current flows in the positive direction of the MOSFET.

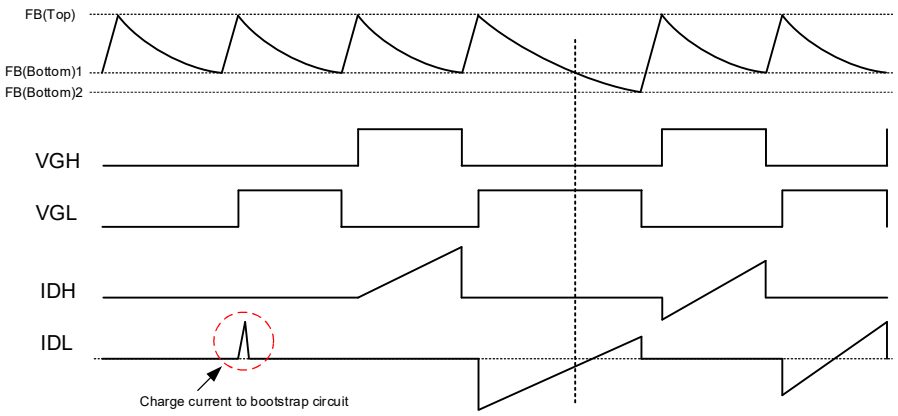


Fig 29. Tss(3) Operation Sequence

(3) During Overcurrent protection function operation, timer intermittent latch stop function

MCZ5216ST has a function of latch-stop after intermittent timer operation during OCP1, OCP2 and di/dt operation. See Table 6 for the timing and conditions for Timer charging, and refer to the timer intermittent latch-stop sequence shown in Fig 30.

When an abnormal condition is detected as shown in Fig 30, the SST terminal is charged. The Timer charging current for charging the SST terminal varies depending on each operation mode, therefore, see Table 6 for the Timer charging current value.

SST terminal has the timer intermittent latch stop function, and under the following condition ① or ②, the SST terminal starts charging further from 2.1V.

① During operation of OCP1 and OCP2
② During di/dt protection operation in Active Standby mode

If the above condition continues and the SST terminal voltage reaches **Vtimer(set) 3.5V** due to the continuous input of the abnormal signal, the mode is intermittent operation mode.
If the abnormal signal disappears during the intermittent operation mode, and if this intermittent oscillation mode is counted twice consecutively, the IC is perfoms by latch-stop.

If the latch is stopped, the latch is released when the Vc2 terminal voltage is equal or less than Latch release voltage (7.0V)

In addition, a reset function for the latch counter is equipped as shown in **Fig 30**. There are two latch counter reset conditions below.

① During SST reaching 2.1V (There is not detection such as OCP, when normal operation mode return.)

② During SST Refresh (during Vc2 ON/OFF)

With this function, the latch counter becomes 0(zero), when the power supply functions normally. If the abnormal state continues, the latch counter is not reset and the timer latch stops after counting twice.

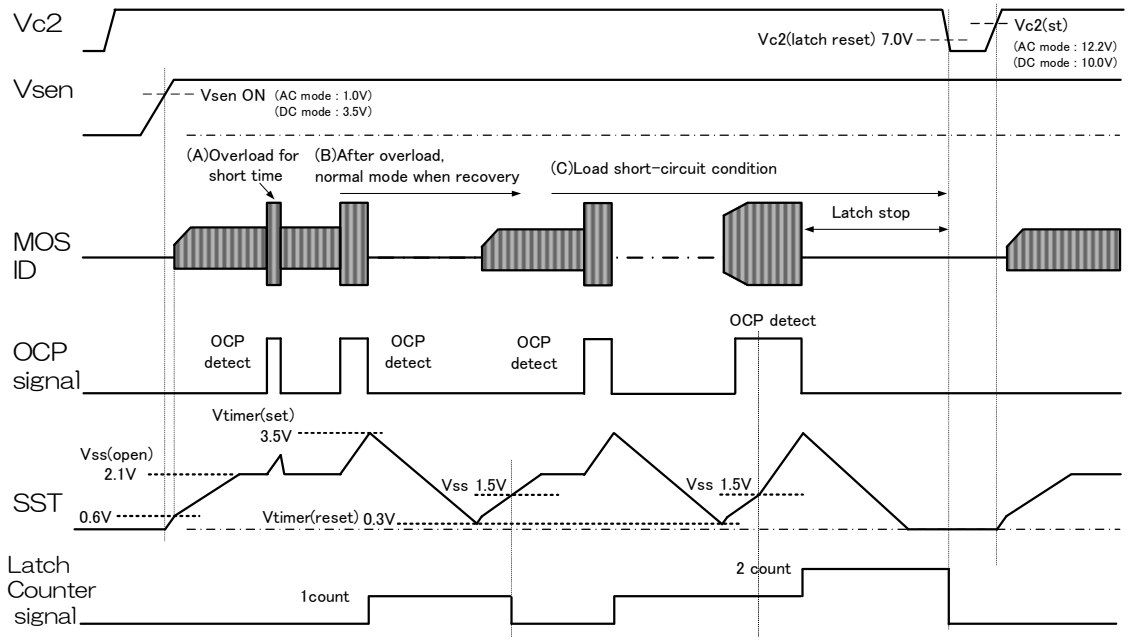


Fig 30. SST Operation Sequence

(4) Latch Stop function

MCZ5216ST is equipped with a latch stop function so that the latch can be stopped in abnormal conditions such as overvoltage on the secondary side. Fig 31 shows an example of the secondary OVP circuit configuration.

The latch function gets valid by lifting the SST terminal to 4.5V from outside. When latch-stop function is valid, oscillation stops.

To release the latch stop, the Vc2 terminal voltage need to be lower than the latch release voltage (7.0V). When the latch is released and the voltage exceeds the Vc2 operation start voltage again, oscillation of the LLC section starts.

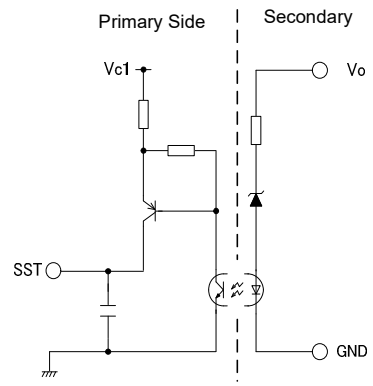
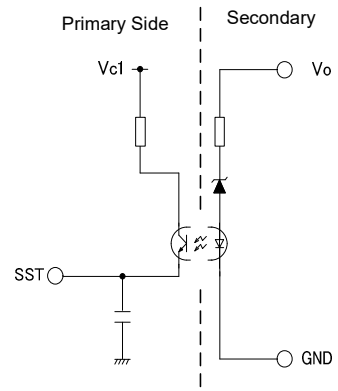
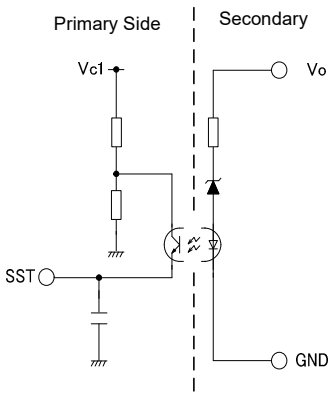
Example ①	Example ②	Example ③
		
It operates fastest among the 3 OVP operations.	If you want to perform OVP operation in the order of several hundred uSec, you need a photo coupler with high CTR.	This configuration is used when OVP operation is possible in the order of several mSec.

Fig 31. Latch Stop function Circuit Configuration example

Table 8. SST terminal threshold value Please check details of each STD value in the characteristics Spec.

Item	Simbol	Condition	STD value	
SST terminal threshold value	Vsst		1.5	V
SST charge current 1	Isst(chg)1	SST=0V	-90	uA
SST charge current 2	Isst(chg)2	SST=1.0V	-30	uA
SST discharge current	Isst(dischg)	SST=1.0V、Vsen=0V	4.0	mA
SST terminal open voltage	Vsst(open)		2.1	V
LLC operation start SST voltage	Vsst(st)		0.6	V
LLC operation stop SST voltage	Vsst(sp)		0.5	V
SST latch stop voltage	Vsst(latch)		4.5	V
Timer threshold value 1	Vtimer(set)		3.5	V
Timer threshold value 2	Vtimer(reset)		0.30	V
Timer charge current 1	Itimer(chg)1		-40	uA
Timer charge current 2	Itimer(chg)2		-1.7	uA
Timer charge current 3	Itimer(chg)3		-40	uA
Latch Release voltage	Vc2(latch reset)		7.0	V
FB charge start voltage 2	Vfb(bottom)2	Tss(3)	2.80	V

2.4.6 Hi-Side Driver Power Supply (VB Terminal)

As shown in **Fig 32**, the floating power supply (VB) for Hi-Side MOSFET drive is generated by the boot strap which uses a diode (Dboot) and a floating smoothing capacitor (Cboot) towards the high voltage side, taking the 12.5V regulator output capacitor at Vc2 as a voltage source.

The potential difference between Low-side and Hi-side by adopting the boot strap circuit due to the external Dboot is sustained at minimum, and provided the stable power supply for driving transiently.

Cboot is used for MLCC, and the recommended value is 0.1u to 1.0uF. And for the Dboot, use a device with a withstand voltage (600V or more) with a high speed and soft recovery characteristics. Our Shindengen **D1NK60 or D1FK60** are recommended (If PFC output voltage is approx. 400V).

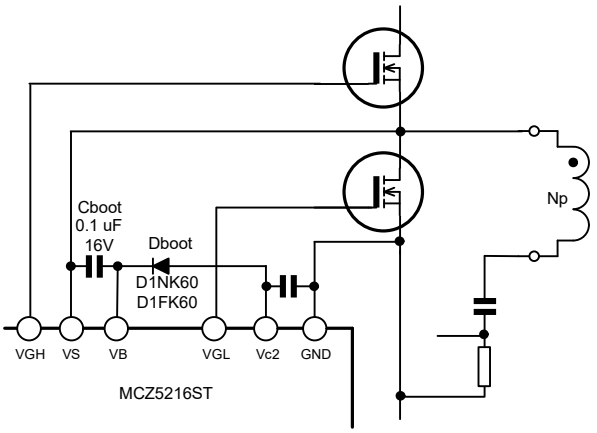


Fig 32. Boot Strap Hi-Side Vcc generated Circuit

Table 9. VB terminal threshold value. Check details of each STD value in the characteristics Spec.

Item	Simbol	Condition	STD value	
Hi-Side Driver operating start voltage	VB-VS(st)		7.5	V
Hi-Side Driver operating stop voltage	VB-VS(sp)		5.5	V

2.4.7 Light load area loss improvement function (ASTBY、Burst Terminal)

Active standby mode and burst mode are controlled according to the ASTBY terminal voltage. See the Table 10 for relationship between each operating mode and ASTBY terminal voltage.

Table 10. ASTBY terminal voltage and each operating mode

ASTBY terminal voltage	Operating Mode	LLC Section
0V ≦ ASTBY ＜ 2.2V	Normal Mode	Symmetric operation
2.2V ≦ ASTBY ＜ 3.0V	Asymmetric linear mode	Asymmetric operation
3.2V ≦ ASTBY ＜ 3.9V	Active Standby mode	Asymmetric operation
4.0V ≦ ASTBY ≦ 5.0V	Burst mode	Asymmetric operation

* Has hysteresis from active standby to burst mode,
Active standby mode → burst mode: ASTBY terminal voltage 4.0V
AST Burst mode → Active standby mode: Switch at ASTBY terminal voltage 3.9V

ASTBY terminal sequence is shown in Fig 33.

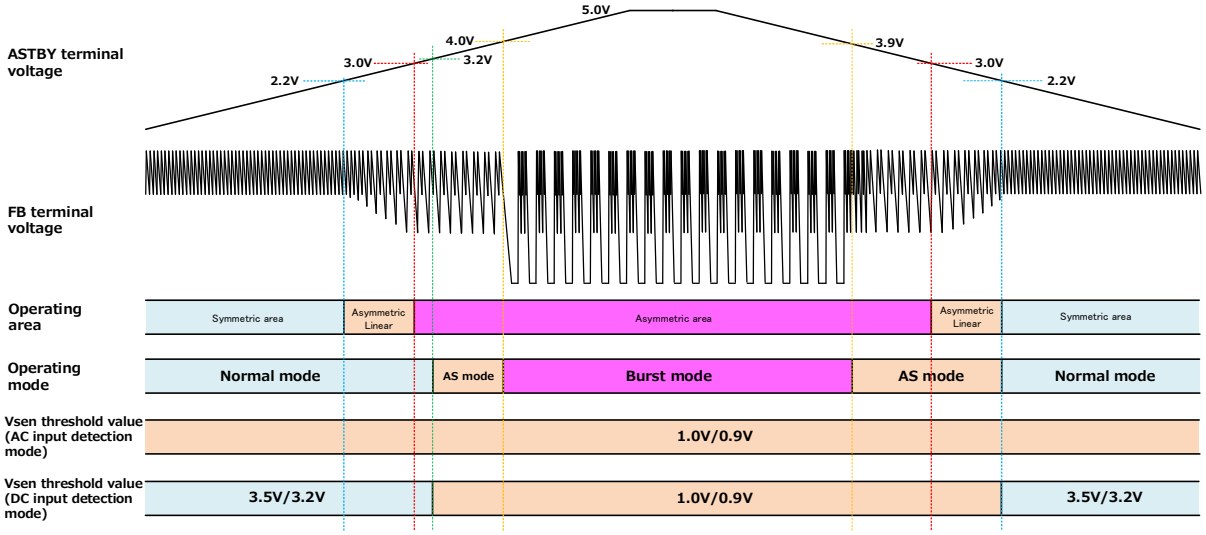


Fig 33. ASTBY terminal sequence.

2.4.7.1 Active Standby Function

The active standby function is a function that can reduce the loss in the light load area with a rated load of approx. 5 to 20%. In the active standby mode, asymmetric operation is performed with the high-side and low-side ON width ratio of approximately 1:2.

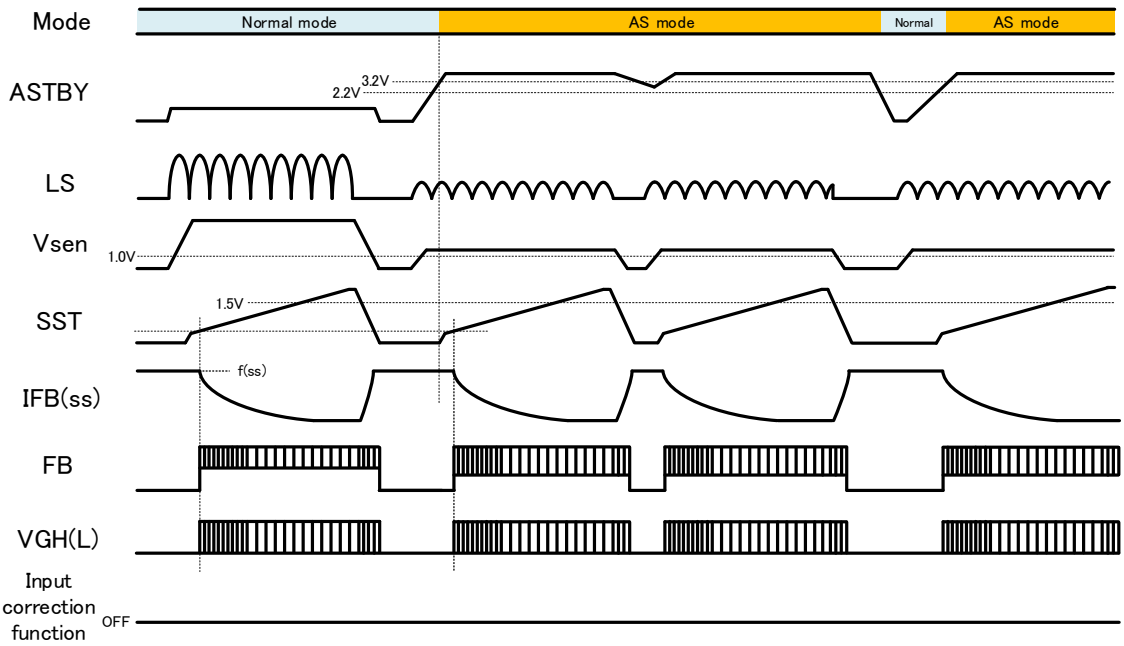


Fig 34. Active Standby Mode Sequence (AC Input Voltage Detection Mode)

See the Fig 34 for detailed operation sequence of each threshold.

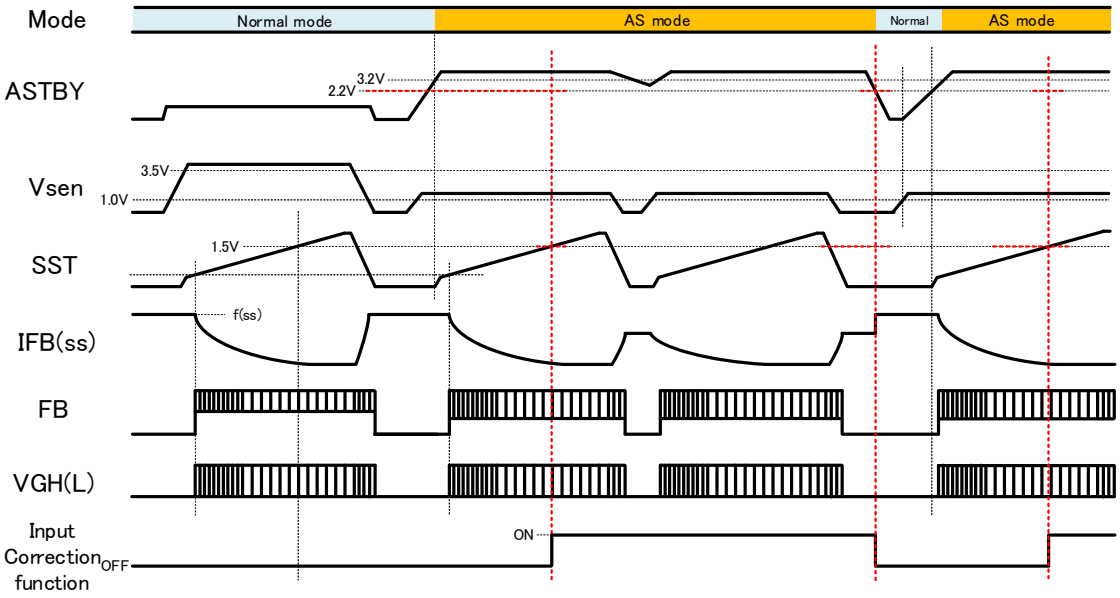


Fig 35. Active Standby Mode Sequence (DC Input Voltage Detection Mode)

The ON width ratio of the high-side and low-side MOSFET changes with the ASTBY terminal voltage. When the ASTBY terminal voltage is 0V, the ON width ratio operates symmetrically with 1:1. When the ASTBY terminal voltage exceeds **Vas(linoff) 2.2V**, the FB charge start voltage **Vfb (bottom)** of the low-side MOSFET decreases as shown in Fig 16, and the on-width of the low-side MOSFET increases to perform asymmetric operation.

The FB charge start voltage Vfb (bottom) changes linearly according to the ASTBY terminal voltage, and ASTBY terminal voltage becomes the maximum ON width ratio when the Vas (linon) 3.0V. The ON width ratio of the high-side and low-side MOSFETs at the maximum ON width is approximately 1:2.

When the ASTBY terminal voltage becomes more than Vas (on) 3.2V, it becomes active standby mode. In the DC input voltage detection mode, Vsen threshold is switched from 3.5V/3.2V to 1.0V/0.9V. In the AC input voltage detection mode, Vsen is always constant and is 1.0V/0.9V.

If the ASTBY terminal voltage is set to less than Vas (off) 2.2V during the active standby mode, the active standby mode is cancelled and the mode switches to the normal mode.

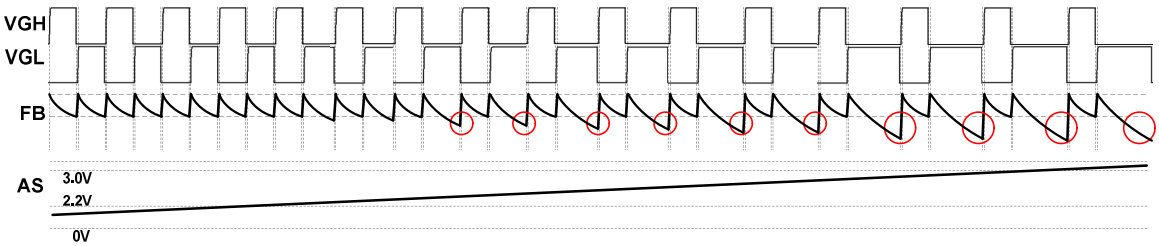


Fig 36. Gate Waveform at AS Linear Operation

In addition, to suppress over (under) shoot when switching between normal mode and active standby mode, MCZ5216ST has a function to control the FB terminal discharge current according to the ASTBY voltage and Vsen voltage.

Fig 37 shows the relationship between the Vsen terminal voltage and the FB discharge current in a schematic diagram, and the Fig 38 shows the FB discharge current sequence when the ASTBY voltage changes.

【AC Input Voltage Detection Mode】

Regardless of the Vsen voltage, the discharge current Ifb(aslin)4 is 170uA, which is the same as Vsen = 4V in Fig 37. Also, as shown in Fig 38, when the ASTBY voltage is between 2.2V and 3.2V, the FB discharge current changes according to the ASTBY voltage. (Change at the line of Vsen = 4V in Fig 38).

When the ASTBY voltage is less than 2.2V, the FB discharge current is 0uA. When the ASTBY voltage exceeds 3.2V, the FB discharge current becomes 0uA.

【DC Input Voltage Detection Mode】

As shown in Fig 37, the FB discharge current changes depending on the Vsen terminal voltage, and when Vsen = 3.2V, it becomes 0uA, and when Vsen = 5V, it becomes 350uA. Also, as shown in Fig 38, when the ASTBY voltage is between 2.2V and 3.2V, the FB discharge current chnages according to the ASTBY voltage.

When ASTBY voltage is less than 2.2V, FB discharge current is 0uA regardless of Vsen voltage. When the ASTBY voltage exceeds 3.2V, the FB discharge current becomes 0uA regardless of the Vsen voltage.

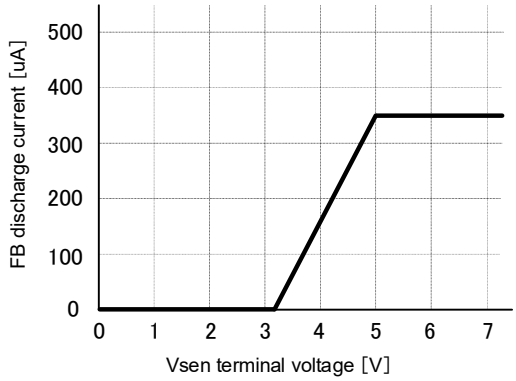


Fig 37. Relation between Vsen voltage and FB discharge current

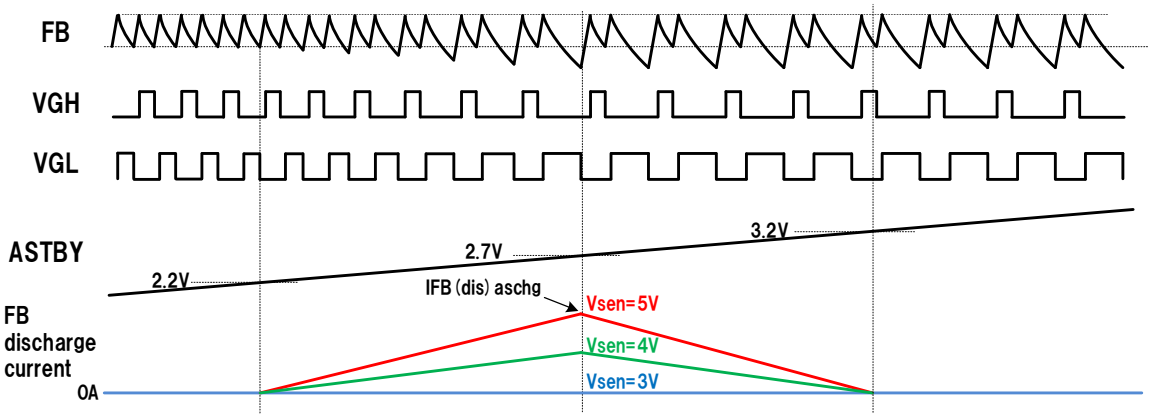


Fig 38. Operation sequence when switching ASTBY (DC input voltage detection mode)

2.4.7.2 Burst Function

The burst function is a function that improves standby power during standby load. The busrt mode is switched by the ASTBY terminal, and oscillation start/stop is controlled by the BURST terminal.

Fig 39 shows a circuit configuration example when using burst mode. Fig 39(a) shows a configuration with two photocouplers, in which the standby ON/OFF section and the output voltage lower limit detection section in burst mode can be controlled independently.
Fig 39(b) shows a case where one photocoupler is used, and one photocoupler can be eliminated.

The burst mode is activated when the ASTBY terminal is 4.0V or higher. To release the burst mode, set the ASTBY terminal to 3.9V or less. In normal mode and active standby mode, the BURST terminal is discharged with a BURST terminal discharge current (400uA). In the burst mode, the discharge of the BURST terminal stops.

In the burst mode, the BURST terminal is lifted by the transformer auxiliary winding voltage Vcc or a voltage divided from an external circuit. When the BURST terminal output stop voltage becomes 2.0V or more, the SST terminal is discharged and the oscillation of the LLC section stops. Next, when the BURST terminal output start voltage drops 1.5V or less, charge of the SST terminal starts and then the LLC section starts oscillating. See Fig 40 for the detailed sequence.

In the burst mode, the SST charging current at soft start is Isst(chg)3 to 90uA. This shortens the soft-start time, so the oscillation time can be shortend during burst operation, and also be contributed to improved standby power.

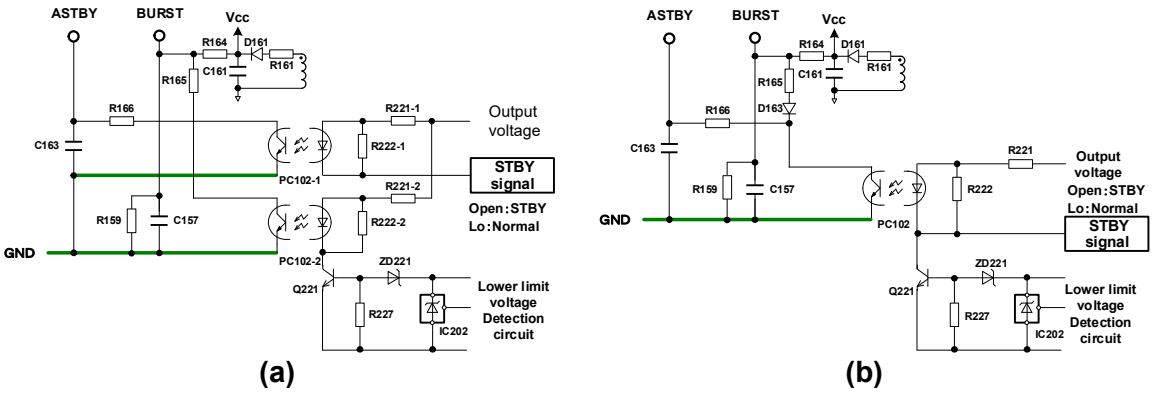


Fig 39 . BURST terminal connection (a) used Coupler 2pcs, (b)used Coupler 1pcs

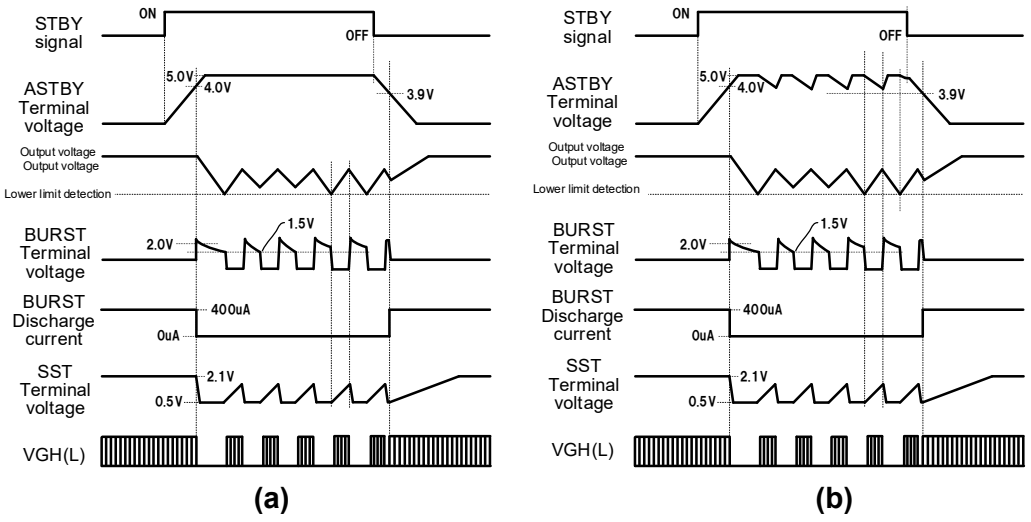


Fig 40. BURST operating sequence (a) Coupler 2pcs, (b)Coupler 1pcs

【fss input voltage correction function (in DC input voltage detection mode)】

MCZ5216ST has a function to change soft start frequency (fss) according to Vsen voltage at the time of burst operation in DC input voltage detection mode. If the Vsen voltage is low as shown in Fig 41(b), fss needs to be lower. This makes it easier to ZVS by varying the current flowing through the MOSFET according to the input voltage fluctuations during the busrt operation.

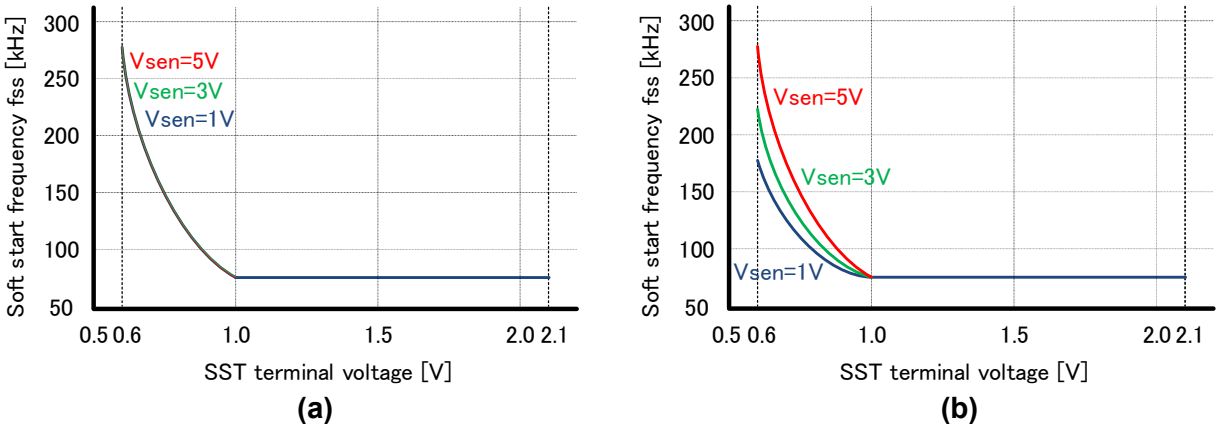


Fig 41. fss input voltage correction (a) AC input detection mode, (b) DC input voltage detection mode

Table 11. ASTBY terminal threshold value. Check detail of each STD value in characteristics spec.

Item	Simbol	Condition	STD value	
AS Linear operation start voltage	Vas(linon)		3.0	V
AS Linear operation release voltage	Vas(linoff)		2.2	V
AS Mode start voltage	Vas(on)		3.2	V
AS Mode release voltage	Vas(off)		2.2	V
ASTBY terminal opean circuit voltage	Vastby(open)		5.0	V
ASTBY terminal charge current 1	Iastby(chg)1	ASTBY=0V	-2.5	uA
ASTBY terminal charge current 2	Iastby(chg)2	ASTBY>Vastby(bston)、ASTBY<Vastby(open)	-5.0	uA
Burst mode start ASTBY terminal voltage	Vastby(bston)		4.0	V
Busrt mode release ASTBY terminal voltage	Vastby(bstoff)		3.9	V
BURST terminal SSTdischarge voltage	Vbst(H)		2.0	V
BURST terminal SSTcharge voltage	Vbst(L)		1.5	V
BURST terminal discharge current 1	Ibst(dis)1	ASTBY<Vastby(bston/off)	400	uA
BURST terminal discharge current 2(Burst Mode)	Ibst(dis)2	ASTBY>Vastby(bston/off)	0	uA
In AS Linear operation FB discharge current 1	Ifb(aslin)1	LS=0V、Vsen=5V、ASTBY=2.7V	350	uA
In AS Linear operation FB discharge current 2	Ifb(aslin)2	LS=0V、Vsen=4V、ASTBY=2.7V	170	uA
In AS Linear operation FB discharge current 3	Ifb(aslin)3	LS=0V、Vsen=3.4V、ASTBY=2.7V	50	uA
In AS Linear operation FB discharge current 4	Ifb(aslin)4	LS>Vls(acon)、Vsen=6V、ASTBY=2.7V	170	uA

2.4.8 Thermal shutdown Protection Function(TSD function)

MCZ5216ST has Thermal shutdown protection function. When this function is operated, LLC oscillation stops. The overheat protection operation start temperature is the operation stop temperature (**TSD: 140℃.min**). There is hysteresis in the overheat protection temperature, and the overheat protection release temperature is released when the **ΔTSD falls 40℃** lower than the operation stops temperature, and returns to normal operation.

Table 12. TSD function threshold value. Check details of each STD value in characteristics spec.

Item	Simbol	Condition	STD value	
Operation stop Temp.	TSD		140	℃
Operation stop/ Return Temp. range	ΔTSD		40	℃

2.4.9 Vc1 Overvoltage Protection Function(Vc1 OVP Function)

MCZ5216ST has a latch stop function when Vc1 terminal overvoltage is applied. If Vc1 terminal voltage exceeds 33.0V(Vc1: ovp latch), the latch stops.
To relase the latch stop, it is necessary for the Vc2 terminal voltage to set 7.0V or less.

Table 13. Vc1 OVP function threshold value. Check detail of each STD value in characteristics spec.

Item	Simbol	Condition	STD Value	
Vc1 Overvoltage Protection Voltage	Vc1(ovp latch)		33.0	V
Latch release Voltage	Vc2(latch reset)		7.0	V

2.5 Reference

2.5.1 When operating from low input voltage

[When operating in AC input voltage detection mode]

In the AC input voltage detection mode, gate output will not start during normal operation unless the Vsen terminal rises to Vsen1 (1.00V).

If you want to operate the LLC from a low input voltage when evaluating the power supply, apply a voltage of 1.5V or more to the LS terminal. Also, when active standby or burst mode works, check the operation with the ASTBY terminal shorted to GND.

However, if the input is turned ON/OFF in this state, resonance may be lost continually, and a heavy load may be applied to the MOSFET, therefore, start up by increasing the input voltage gradually under no load condition. In addition, the operation from the low input voltage described above should be used only for studying power supply evaluation.

[When operating in DC input voltage detection mode]

In DC input voltage detection mode, gate output will not start during normal operation unless the Vsen terminal voltage rises to 3.5V(Vsen5).

If you want to operate LLC from low input voltage at the time of power supply evaluation etc., please apply the voltage of 3.5V or more to Vsen terminal with LS terminal shorted to GND. Also, when active standby or burst mode works, check the operation with the ASTBY terminal shorted to GND.

However, if the input is turned ON/OFF in this state, resonance may be lost continually and a large load may be applied to the MOSFET, therefore, start up by increasing gradually the input voltage with no load condition. In addition, the operating from the low input voltage descreibed above should be used only for studying power supply evaluation.

2.5.2 When the Vin terminal is not used

If the Vin terminal is not used, short the Vin terminal to GND or open the terminal.
For Vcc supply of MCZ5216ST, apply voltage to Vc1 terminal. It is recommended that the capacity of the capacitor between Vc2 and GND be around 4.7u to 47uF. Use the unused condition of Vin terminal only in the DC input voltage detection mode.

2.5.3 When not using Active standby or Burst mode.

If neither active standby nor burst mode is used, short the ASTBY terminal to GND. Also, short the BURST terminal to GND.

If only the burst mode is not used, short the BURST terminal to GND.

3 Determination of peripheral circuit constants.

3.1 Input monitoring section design in AC input voltage detection mode (LS, Vsen terminal)

【AC input voltage detection mode】

Fig 42 shows an example of LS and Vsen terminal connection. Use the connection example in Fig 42 when you want to use the X-capacitor discharge function after AC OFF.

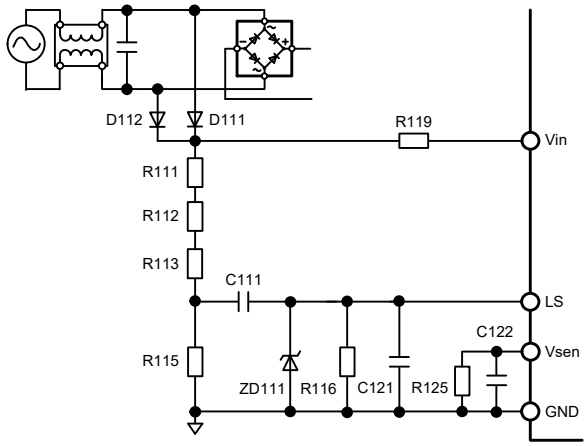


Fig 42. LS/Vsen terminal connection

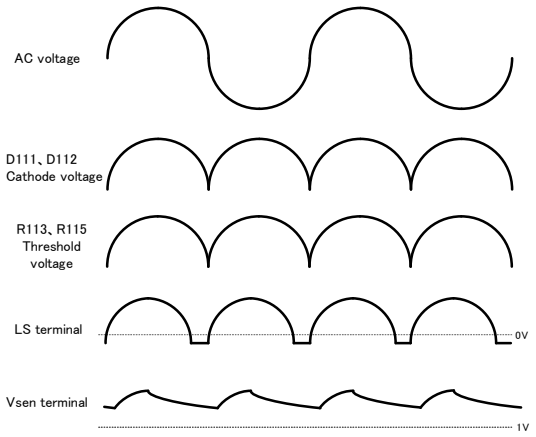


Fig 43. LS/Vsen terminal waveform

Generate a voltage converterd by the LS/Vsen conversion ratio from the voltage applied to the LS terminal inside the IC. Compared the Vsen terminal with the voltage generated inside the IC, if the Vsen terminal voltage is lower than the voltage generated inside the IC, charge the Vsen terminal so that it can be the same voltage generated inside the IC. The converson ratio for LS/Vsen is 1.20, and the voltage shown in Formula (1) is applied to Vsen terminal.

$$\mathrm{Vsen} = \frac{\mathrm{VLS}}{1.2}[\mathrm{V}] \quad \cdots\textbf{(1)}$$

The Vsen terminal connects the capacitor (C122) and the discharge resistor (R125). Vsen terminal voltage is smoothed by C122 capacitor. By discharging the Vsen terminal with R125, when the LS terminal voltage at AC OFF falls, the Vsen terminal voltage operation is stopped by setting the Vset terminal voltage at 0.9V or less.

Fig 43 shows the waveforms of LS terminal voltage and Vsen terminal voltage. The operation start/stop time at AC ON/OFF changes depending on the C122 and R125 constants. It is recommended that the initial constant of C122 be around 0.01uF and R125 be about 470Kohm respectively.

Regardless of the oscillator operation mode, the Vsen terminal threshold value is 1.00V/0.90V. Therefore, the start/stop points changes depending on the resistance partial voltage value connected to the LS terminal. Also, the voltage generated at LS terminal varies depending on the value of the rectifier capacitor value after the Y capacitor and bridge diode, therefore, please set it by referring to the design example below.

Fig 44. shows an example of LS/Vsen terminal design assuming AC100V to AC240V(W/W) and 50/60Hz.

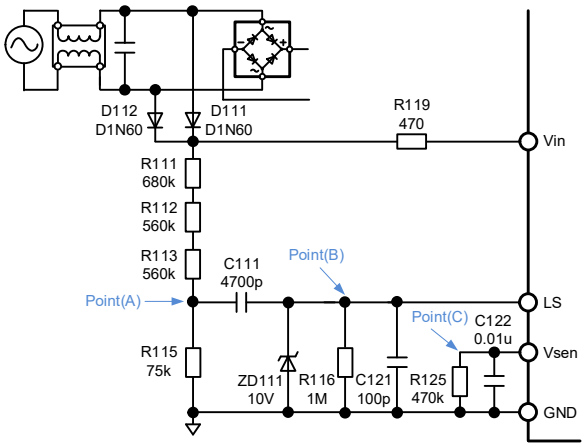


Fig 44. LS/Vsen terminal design

D111 and D112 are for rectifying AC voltage. For AC100V to AC240V and 50/60Hz, general rectifier diode can be used and Shindengen D1N60 is recommended. Refer to the Table 1 and select the resistor (R119) to be connected to the Vin terminal.

C111 is a capacitor that cuts the DC composition. By connecting this capacitor, the voltage is supplied to the LS terminal at the time of AC ON. When the voltage generated at the point(A) after AC OFF becomes DC, the LS terminal voltage decreases by cutting DC composition. It is recommended that C111 be around 4700pF.

The current flowing to C111 is rectified by C121 and discharged by R116. And ZD111 is a Zener diode for voltage clamp and negative voltage clamp applied to the LS terminal. When operating at 50/60Hz, it is recommended that R116 be around 1Mohm, and C121 be about 100pF. In addition, insert a low-leakage Zener diode of 10V or less into ZD111.

The current flowing through R111 - R113 is determined by the current flowing through R115 and the current flowing through C111. Since it is necessary to flow several uA to C111, R111 - R113 should select a resistance value that allows current to flow more than 10 times. Under these conditions, the total resistance of R111 - R113 is recommended to be around 2Mohm.

First, consider the case where C111 is open at AC100V. The voltage generated at point (A) when C111 is open is point (A)' . At the point (A)', the divided voltage of R111 - R113, and R115 is generated. In case of AC100V, the voltage of (141V x 75Kohm)/(1.8Mohm + 75Kohm) = 5.64V at point (A). In this case, the current flowing through R115 is 5.64V/75Kohm = 75.2uA.

Next, assuming that a peak voltage of 5.64V is generated at point (A)", voltage point (B) generated at the LS terminal by the current flowing through C111 when C111 is connected is defined as point (B)". Under this condition, approximately half of the voltage is applied to point (B), so the LS terminal becomes 2.82V. Therefore, the current flowing to C111 is 2.82V/1Mohm = 2.82uA.

The current that actually flows to point (A) is 75.2uA - 2.82uA = 72.38uA, and the voltage value is 5.43V. Therefore, at the point (B), a slightly small value is output, which is approxmately 5.43V/2=2.72V. Based on these values, adjust the Vsen terminal voltage so that it does not fall below 0.9V at the lower limit of the expected AC input voltage.

The above values are the intial values, so please check with the actual equipment finally.

3.2 Input monitor design in DC input voltage detection mode (Vsen terminal)

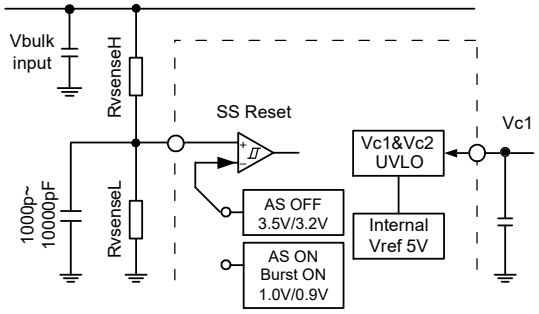
【DC input voltage detection mode】
Vsen terminal threshold value is 3.5V/3.2V (Normal mode)
1.0V/0.9V (Active standby mode, Burst mode)

The sink current of Vsen terminal needs 0.2uA, it is recommended to design so that about the current (around 20uA) can flow in order not to be affected by the sink current. High potential side Vbulk detection resistor (RvsenseH) is recommended about 2Mohm (When the PFC output voltage is about 400V.)

Connect a capacitor of about 1000p - 10000pF between Vsen terminal and GND for noise absorption.

Calculate the initial value RvsenseL(init) from the desired Brown Out protection voltage threshold Vbulkreset by Formula (2), and after that, substitute the real constant in Formula (3) and check the value of Vbulkreset finally.

In the active standby mode, the Vsen threshold changes, so substitute a real constant into Formula (4), and check the desired Vbulkreset (AS ON).



$$R_{VsenceL\,(init)} = \frac{3.2 \times R_{VsenseH}}{V_{bulkreset} - 3.2} \quad [\Omega] \qquad \cdots (\mathbf{2})$$

$$V_{bulkreset} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 3.2 \quad [V] \qquad \cdots (\mathbf{3})$$

$$V_{bulkreset\,(AS\,ON)} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 1.0 \quad [V] \qquad \cdots (\mathbf{4})$$

Fig 45. Vsen terminal internal structure (at DC Input Detection Mode)

3.3 Oscillation Control Section (FB terminal)

The oscillation frequency of the LLC section is controlled by the FB terminal. The FB terminal determines the dead time, initial, maximum, and minimum oscillation frequencies. Since the gate ON/OFF timing is determined by the charging/discharging timing of the FB terminal, connect the capacitor and resistor connected to the FB terminal as close to the IC as possible.

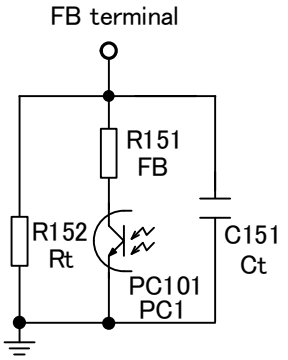


Fig 46. FB terminal Connection Diagram

Connect the Rt resistor and FB resistor shown in Fig 46 to the FB terminal in addition to the Ct capacitor.

Dead time and soft start frequency are determined by the capacitance of Ct capacitor. See 3.3.1 for details.

The minimum oscillation frequency is determined by the Rt resistor, and the maximum oscillation frequency is determined by the Rt resistor and the FB resistor.

See 3.3.2 and 3.3.3 for how to determine Rt resistance and FB resistance.

3.3.1 Adjustment of dead time and soft start frequency fss (adjustment of Ct capacitor)

The dead time and the soft start frequency fss vary depending on the capacitance of the Ct capacitor, as shown in the characteristic diagrams in Fig 47 and Fig 48

Select the capacitance of Ct capacitor according to the oscillation frequency during steady operation and also the gate capacity/switching characteristics of the MOSFET.

As an initial value, when using Shindengen MOSFET(P15F50HP2) at a frequency of 100KHz during normal operation, the capacitance of the Ct capacitor should be about 1500pF. When using a 15A class super-junction MOSFET at a frequency of 300KHz during normal operation, the capacitance of the Ct capacitor should be 820pF. Since the desired dead time varies depending on the resonance conditions, and etc., the above values should be used as initial values and finally adjusted with the actual equipment.

When designing the Ct capacitor within the range of 100K to 500KHz, we recommend about 470p to 2200pF. If the capacitance of the Ct capacitor is too small, the overshoot and understoot during charging and discharging will increase, so consider about 470pF as the minimum value. It is possible to increase the capacitance of the Ct capacitor to more than 2200pF, but since the soft-start frequency decreases, the current peak of the MOSFET tends to increase during startup. When increasing the capacitance of the Ct capacitor, check if there is no problem with power supply operation.

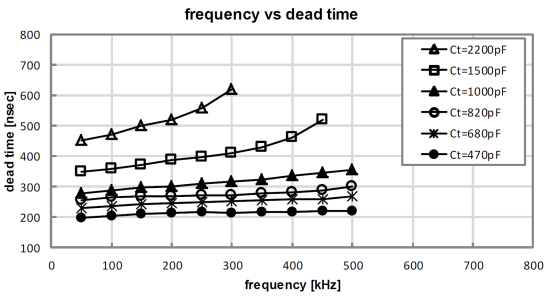


Fig 47. Correlation for Frequency vs Dead-Time

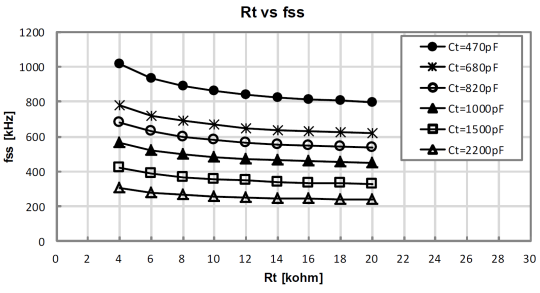


Fig 48. Corrleation for Rt vs Fss

3.3.2 Min Oscillation Frequency(=fmin) Adjustment(Adjustment of Rt restriction Resistance)

The minimum oscillation frequency fmin is determined by the Rt resistance value connected to between FB terminal and GND.

Check the characteristic diagram in the power supply specification for the relationship between Rt resistance value and the oscillation frequency. From the characteristic diagram, check fmin from the Formula (5)-(7) after selecting the Rt resistance value to be the desired fmin.

The tcharge is the dead time period and tdischarge is the period of the one-side gate. VFB(top) is the FB charge stop voltage, and VFB(bottom) is FB charge start voltage.

The response delay is not included in the standard value stated in the specification, therefore, overshoots and undershoots actually occur due to the oscillation frequency. First, as soon as the constant is determined in the Formula (5)-(7), adjust the oscillation frequency measued actually by referring to the characteristic diagram of the power supply characteristics specification.

If fmin is set too low against the oscillation frequency during normal operation, the OCP and di/dt may be masked, which may not be detected by FB mask voltage as the oscillation frequency becomes too low during over-load and load-short-circuit. When changing fmin, please check if OCP or di/dt is detected during load-short-circuit.

$$t_{charge} = \frac{Rt \times Ct \times VFB_{(top)}}{Rt \times 11 \times 10^{-3} - VFB_{(top)}} - \frac{Rt \times Ct \times VFB_{(bottom)}}{Rt \times 11 \times 10^{-3} - VFB_{(bottom)}} \ [sec] \cdots (5)$$

$$t_{discharge} = -Rt \times Ct \times \ln \frac{VFB_{(bottom)}}{VFB_{(top)}} \ [sec] \cdots (6)$$

$$f_{min} = \frac{1}{2 \times \left(t_{charge} + t_{discharge}\right)} \ [Hz] \cdots (7)$$

3.3.3 Max Oscillation Frequency(=fmax) adjustment (Adjustment of FB Limit Resistance)

The maximum oscillation frequency fmax is become when the photocoupler is turned on at max, so the resistance to determine the maximum oscillation frequency is determined by the value when it is assumed that the Rt resistor and FB resistor are connected in parallel.

For example, let us explain to you about the case of Ct=820pF as a example. If the minimum oscillation frequency is approx. 150KHz and maximum oscillation frequency is approx. 300KHz, the Rt resistance is 11Kohm due to the characteristic diagram.

In addition, the maximum oscillation frequency from the characteristics diagram, the combined resistance is approx. 5.5Kohm, therefore, if Rt resistance is 11Kohm, FB resistance is about 10Kohm. Finally, determine the constant after confirming the maximum - minimum oscillation frequencies with the actual equipment.

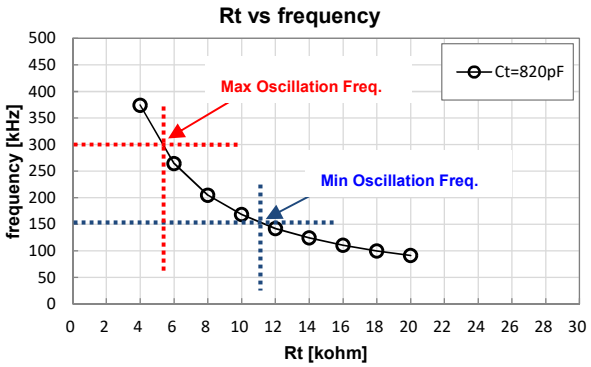


Fig 49. Max/Min Oscillation Frequency Setting

3.4 Timer charge-time adjustment at soft start and abnormality (SST terminal)

The SS charge current Isst(chg)2 to the SST terminal is 30uA on soft-start operation. SST voltage reaches the threshold Vss at 1.5V or more, timer charge becomes available during OCP operation, therefore, the soft start time is calculated by the time until 1.5V(=SST).

If the time til SST voltage reaches 1.5V from during the gate output being started at SST voltage (0.6V) is Tss, it is obtained as shown in Formula (8). During soft start, for the relationship between SST terminal voltage and oscillation frequency, see the characteristic diagram in the characteristic specification document. When there is no abnormality such as OCP, the SST terminal voltage rises up to 2.1V.

$$t_{ss} = \frac{0.9 \times C_{ss}}{30 \times 10^{-6}} \quad [\text{sec}] \quad \cdots(8)$$

Also, time charge current Itimer (chg)1 to SST terminal at detection of di/dt for OCP1 operation and active standby operation is 40uA.

After SST voltage stabilizes at 2.1V, the SST terminal voltage increases due to OCP1 operation, and the time (Ttimer) reaching til SST(3.5V) is calculated as shown in Formula (9)

$$t_{timer} = \frac{1.4 \times C_{ss}}{40 \times 10^{-6}} \quad [\text{sec}] \quad \cdots(9)$$

The charge current to SST terminal at OCP2 operation varies depending on CSO terminal voltage. Timer charge current Itimer(chg)2 when CSO < 3.6V is 1.7uA. The time reaching til SST (3.5V) is calculated as shown in Formula (10).

$$t_{timer} = \frac{1.4 \times C_{ss}}{1.7 \times 10^{-6}} \quad [\text{sec}] \cdots(10)$$

Timer charge current (chg)3 is 40uA when CSO≧3.6V, the time (Ttimer) reaching til SST(3.5V) is calculated as shown in Formula (9).

And during the intermittent operation after reaching SST (3.5V), timer discharge current Itimer(dischg) from SST terminal is 6uA.

Stop period of oscillation during intermittent operation is released, when SST voltage decreases to Vtimer (reset) by 0.30V.
Therefore, the stop period of oscillation Ttimer (Stop) at intermittent operation time is calculated as shown in Formula (11).

$$t_{timer\ (stop)} = \frac{3.2 \times C_{ss}}{6.0 \times 10^{-6}} \quad [\text{sec}] \quad \cdots(11)$$

3.5 Over-Current-Protection (OCP, di/dt), Adjustment (CS, CSO terminal)

Over-current detection of the LLC section is measured by CS terminal.

The current Ipk flown into the resonance capacitor C123 is converted into a voltage by the detection resistance R141, and then the voltage divided by R143 and R144 is detected by the CS terminal.

In addition, since 100uA of the CS terminal current flows, it is recommended that R143 be approx.10 to 47ohm.

Due to avoiding malfunction by switching noise, insert a filter capacitor for C141. It is recommended that the filter capacitor be of approx.0.01uF.

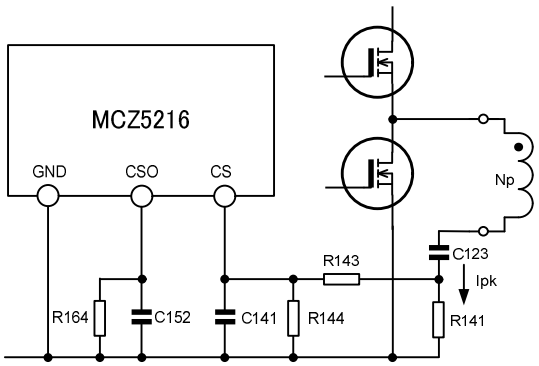


Fig 50. Over-Current-Detection Circuit

Overcurrent protection function becomes +/-0.500V at OCP1 and +/-0.350V at OCP2, therefore, OCP2 operates first.

Supposed the resonance capacitor current is as Ipk during the desired OCP2 operation, the voltage detection resistance R141 needs to be a constant that satisfies Formula (12). R143 and R144 are calculated from Formula (13). For the R143 constant, get it by setting a constant of R144 as around 10ohm to 47ohm. As OCP2 detection threshhold value is reduced to a maximum of 0.25V due to the input voltage correction function of OCP2 stated in 2.4.4, calculate by replacing the value (0.35) with a suitable value into Formula (12) to (14).

Finally, check if the desired Ipk value is obtained by entering a real constant in Formula (14).

$$R141 > \frac{0.35}{Ipk} \qquad [\Omega] \quad \cdot\cdot\cdot (12)$$

$$R144 = \frac{0.35 \times R143}{Ipk \times R141 - 0.35} \qquad [\Omega] \quad \cdot\cdot\cdot (13)$$

$$I_{pk(cal)} = \frac{R143 + R144}{R144 \times R141} \times 0.35 \qquad [A] \quad \cdot\cdot\cdot (14)$$

Connect a capacitor C152 and a registor R164 to the CSO terminal. Vary the oscillation frequency by charging CSO terminal when OCP1 and OCP2 operating. See Table 6 for CSO terminal charge current during operation of OCP1 and OCP2. Adjust the capacitor connected to the CSO terminal after confirming the response with the actual device. The initial value for C152 is from 1000p to 1.0uF, and for R164 is from 10K to 100Kohm. If you want to latch the intermittent-timer safely by narrowing down on the oscillation frequency early when the load is short-circuited, speed up the response by setting 1000pF at C152, 100Kohm at R164, or by just open. In this case, check if output voltage does not lower by detecting the OCP2 in the normal operating range as the response gets faster when OCP2 being detected.

3.6 Circuit Constants Setting when using Active Standby

Fig 51 shows a circuit configuration example when using active standby.

ASTBY terminal voltage will be active stanby mode at more than 3.2V. When ASTBY terminal voltage rises at more than 4.0V, burst mode is activated, therefore, set the ASTBY voltage on the active standby mode at more than 3.2V up to lower than 4.0V.

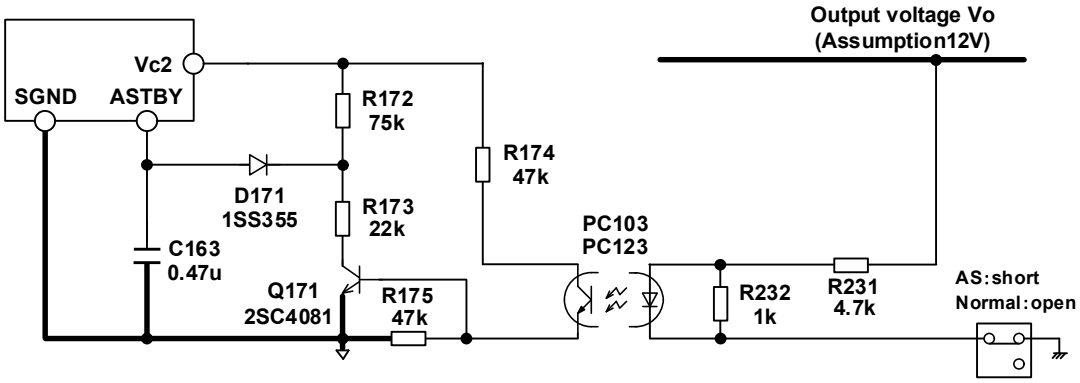


Fig 51. Active Standby Circuit

Fig 51 show you another circuit example that becomes standby mode by short-circuit between secondary side SW and GND. When secondary side SW and GND are short-circuited, Q171 turns on due to conducting photocoupler of PC103. Therefore, the added value of Vf of D171 to the voltage determined by the divided resistance of R172 and R173 generates at the ASTBY pin voltage. Since the foward current flowing through D171 is 1mA or less, check the diode Vf at that time.

If the revers current of D171 is large, the ASTBY voltage maiy increase even at normal mode, therefore, select a low reverse current type of the diode like 1uA or less when selecting D171.

3.7 Circuit Constants Setting when using Burst.

Fig 52 and 53 show you the circuit configuration examples when using burst-mode. Both are assumed that 5V output is perfomed at 12V by DC/DC.

Lower-limit of 12V output voltage at burst mode is determined by resistance value of R223 and R224. The lower-limit of output voltage becomes 7.84V when the reference voltage of IC202 setting at 2.5V, at 47Kohm by R223, and 22Kohm by R224.

The BURST terminal discharge current during normal active standby is 400uA, therefore, if the resistance values for both R159 and R164 is too small/low, the BURST terminal voltage rises, and then intermittent operation may occur. R159 should be approx. 15Kohm, and adjust the burst cycle with R164 resistance value. The busrt terminal voltage is determined at more than 1.5V when auxiliary winding voltage is around 10V, by R164 considering Vc2 UVLO.

R165 and C157 are determined considering the burst cycle. For D163, select a diode with a low reverse current type in the same way as that of D171 in Section 3.6.

R166 shown in Fig. 52 needs to be lower than 1.8V in normal mode.
For example, supposed the coupler is short-circuited thoroughly and R166 is 470Kohm, according to calculation, the ASTBY charge current is 2.5uA so the ASTBY terminal voltage rises up to 1.18V.
If the load is increased during the burst, the number of times for turn-on of PC102 increase, and discharge time of ASTBY terminal become longer. However, in case the discharge current becomes larger than ASTBY charge current, the burst mode may become unlocked by ASTBY terminal voltage lower. If the burst cycle may become shorter, use the circuit example of Fig. 53.

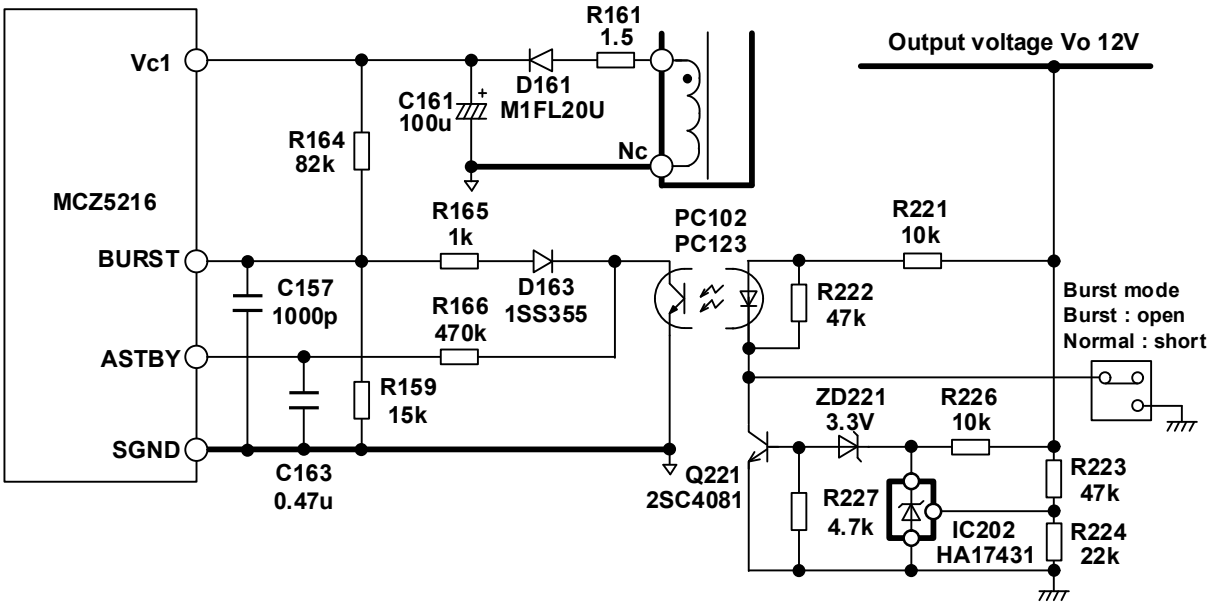


Fig 52. Active Standby Circuit (in case of using 1pcs of Coupler)

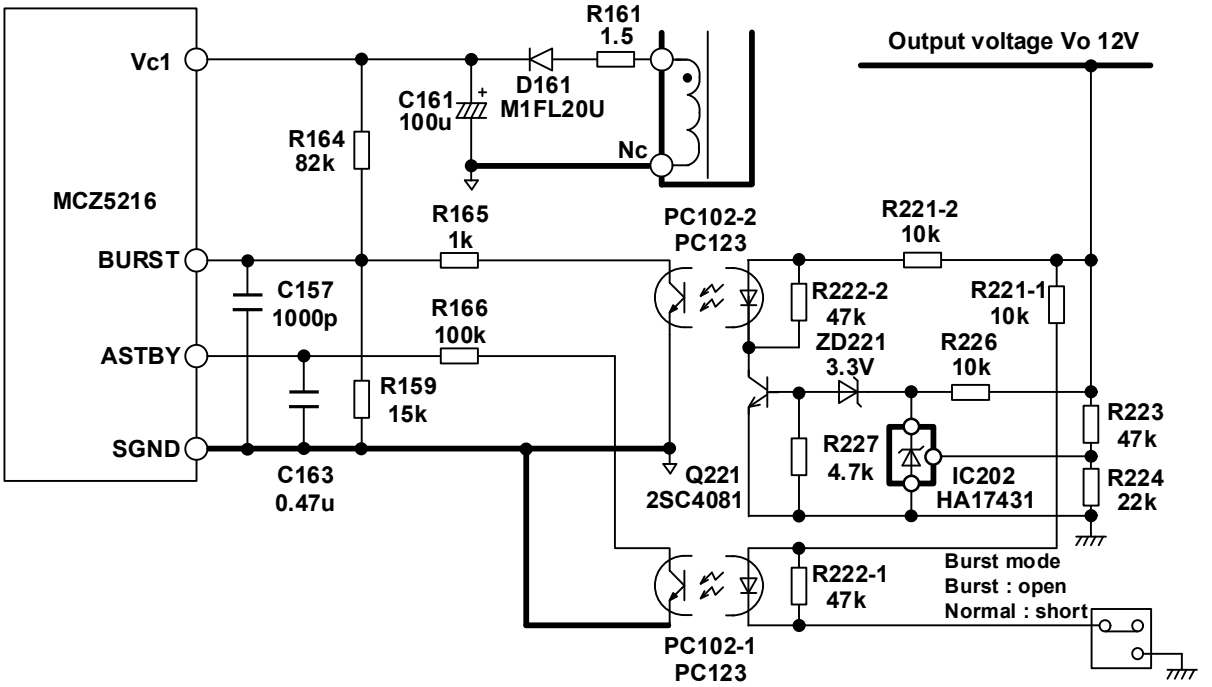


Fig 53. Active Standby Circuit (in case of using 2pcs of Coupler)

4 Pattern Layout of Peripheral of IC

4.1 Caution of Pattern Layout of peripheral of IC

The pattern layout of the switching power supply board affects the power supply characteristics. So MCZ5216ST switches high voltage and large current, great care is required when laying out circuit pattern.

To minimize the occurrence of the noise due to the inductance composition of pattern, it is important for pattern design of the main circuit to make as thick and short as possible. And be sure to wire the pattern of control system so that neither electric field nor magnetic field will be influenced.

Please refer to the precautions for each major item

① Main Current Path Wiring

Connect the power system GND, (separating it from main current line returning to input capacitor), from source of low-side MOSFET to IC's GND. And also connect signal GND and power GND to the IC GND terminal closely by separating signal GND from power GND.

② Signal Line Wiring

Components such as capacitors and resistors for signal lines (FB terminal, CS terminal, Vc 1/2 terminal and etc) should be connected as close to the IC as possible due to preventing malfunction.

If the both pattern for between the FB pin photocouplers and the return from the photocoupler is close to the pattern of the high-voltage switching line (e.g., resonant capacitor), the FB pin voltage may affect the high-side/low-side gate output. Arrange the pattern as far away from high voltage lines, resonance capacitors, and transformers as possible.

If both patterns for between the CS terminal from detection resistance are close to abovementioned high voltage switching line, CS terminal voltage may fluctuate and then the malfunction may occur because CS terminal is for overcurrent-detection. Like the FB terminal, arrange the pattern as far away from the high voltage line, resonance capacitor, and transformer as possible.

③ Gate Output Line Wiring

The gate charge/ discharge current has a sharp spike shape, and the surge voltage due to parasitic L/C of the pattern and components may cause unstable operation of the IC. Therefore, separate the drive loop and the signal GND.

④ High Voltage Line Wiring

The boostrap smoothing capacitor should be placed as close to the IC as possible, and the VS line connected to source of high-side MOSFET should be connected directly to source of the MOSFET by separating from main switching current line.

【Caution when ovserving waveform】

(a) When measuring each MOSFET Current(A)

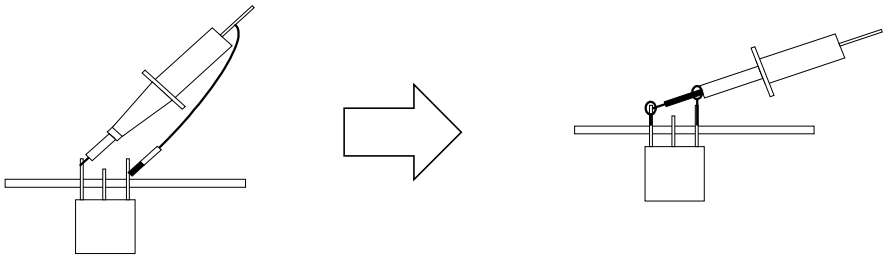
In order to suppress the influence of the parasitic impedance of the lead-wire, please use a wire with a withstand voltage of 500V or more, and connect it with as short wiring as possible.
Use a DC probe as well.

(b) When measuring High Potential Side Voltage.

Pay attention to the probe withstand voltage because LLC MOSFET, resonance capacitor on the primary side, and transformer are high voltage. And also due to the fact that terminals for LLC high-side MOSFET, VGH, VS, and VB are of floating circuit, so use a calibrated differential probe when observing the floating section.

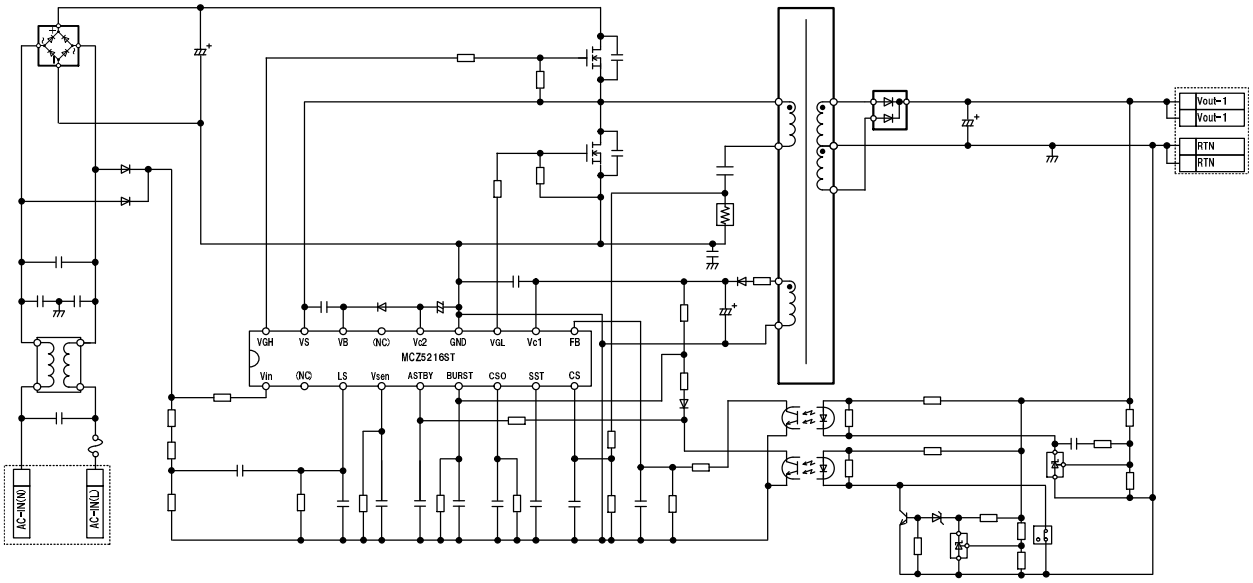
(c) When measuring Low Potential Side

When observing low-voltage/high-frequency teminals such as the FB terminal, swiching noise may be superimposed depending on the probe GND, and also a waveform different from the actual waveform may be observed. If the surge voltage composition affects the measurement, do not use the lead for the GND of the voltage proble, and set a pin at the measurement point as shown below.
Especially, between FB and GND is the terminal that determins the oscillation frequency of the LLC section, and be careful on connecting the GND, when observing the probe to avoid the influence of connecting the probe.

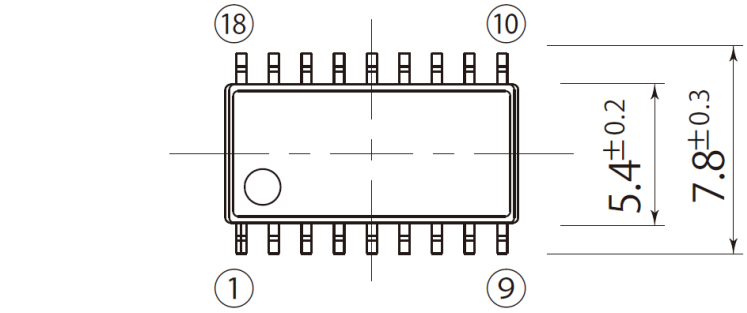


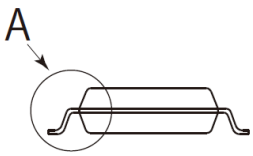
5 Circuit Example

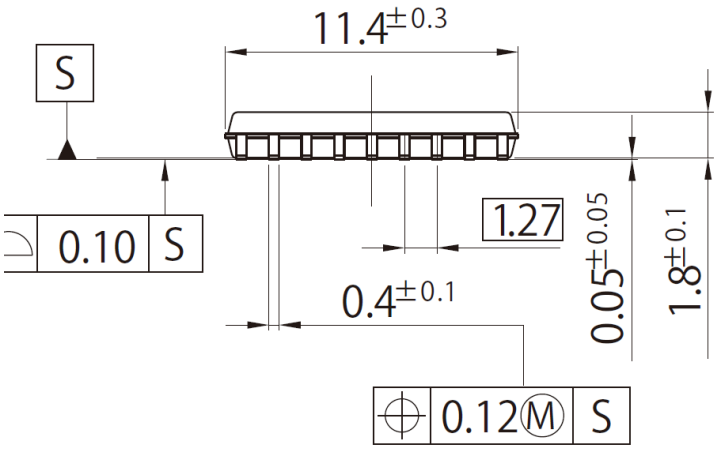
5.1 Basic Circuit

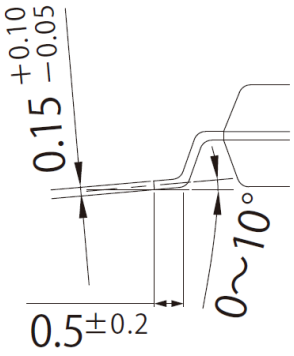


6.1 SOP18 (MCZ5216ST)

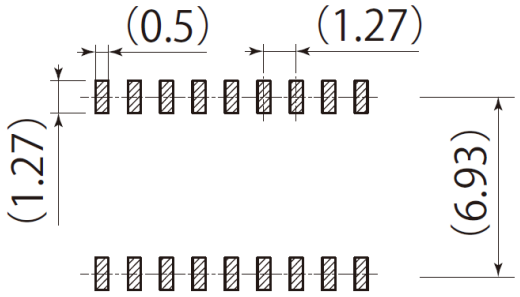








Detail A



Referential Soldering Pad

Notes: