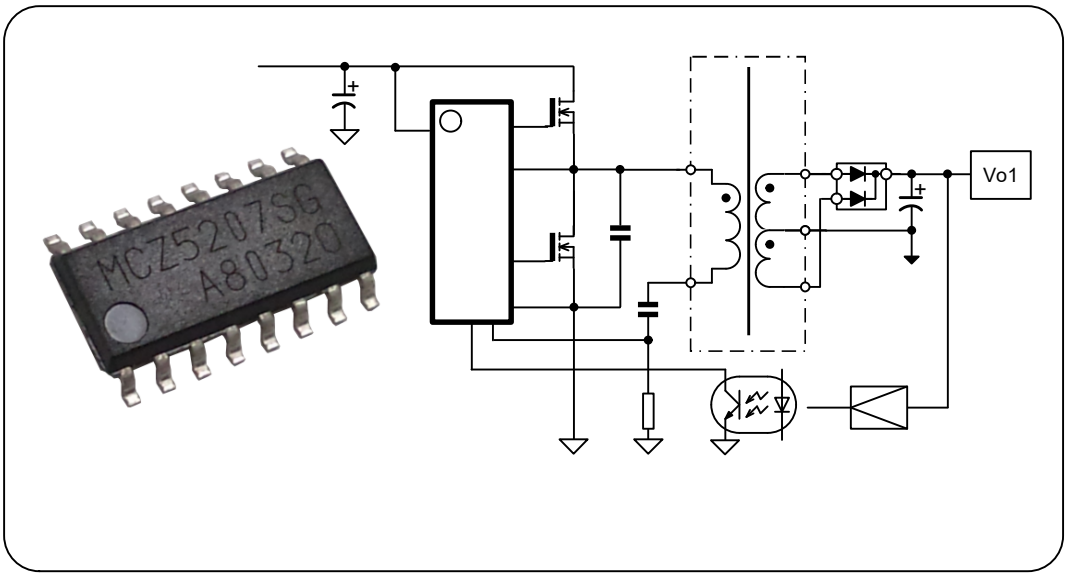
CAT.No. 1H0100-2E

MCZ5207SG APPLICATION NOTE **Jan.2019 Ver1.1**

LLC
Current resonant bridge controller

MCZ5207SG



Shindengen Electric Manufacturing Co., Ltd.

MCZ5207SG
Application Note

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1 General description

MCZ5207SG is an advanced symmetric LLC current resonant mode controller for bridge converter. Built-in high voltage direct gate drivers, control circuit and optimized protections allow simplified and space/cost-saving design of power supplies for :

- Large screen flat panel TVs (PDP / LCD)
- Document equipment
- High power adapter
- CVCC high power LED lighting
- High power standard PSU
- High power Audio Amp

1.1 Features

1. Robust 600V direct gate driver.
2. Optimized protections (OCP/burst/Timer delayed latch/Thermal) for LLC converter.
3. Bidirectional resonant current sensing.
4. Bidirectional **capacitive mode protection**.
5. Vcc supply up to 35V with 12.9V/8.7V UVLO .
6. Built-in voltage regulator of 10.5V for gate driver.
7. Independent UVLO for High side/Low side Gate drive VDD.
8. **Safe soft starting function** to prevent MOSFET didt stress.
9. Brown Out protection
10. Resonant peak current stabilized **frequency clamp OLP**. ***NEW***
11. **Active stdby function** to improve light load efficiency. ***NEW***
12. Less than 100mW no load consumption is possible with **burst mode operation**. ***NEW***
13. **Latching protection** with external signal is possible. ***NEW***

1.2 Block diagram（SOP16）

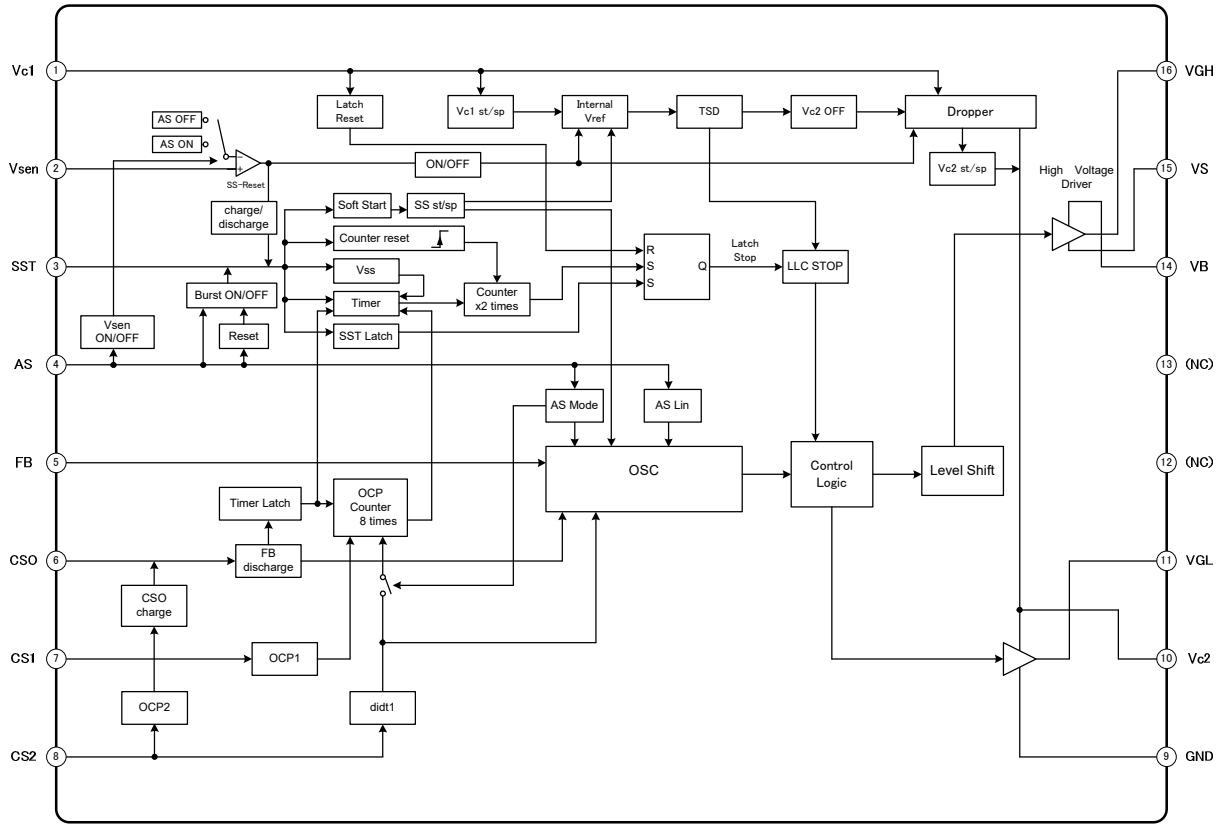


Fig 1 . MCZ5207SG internal block diagram

1.3 Pin assignment

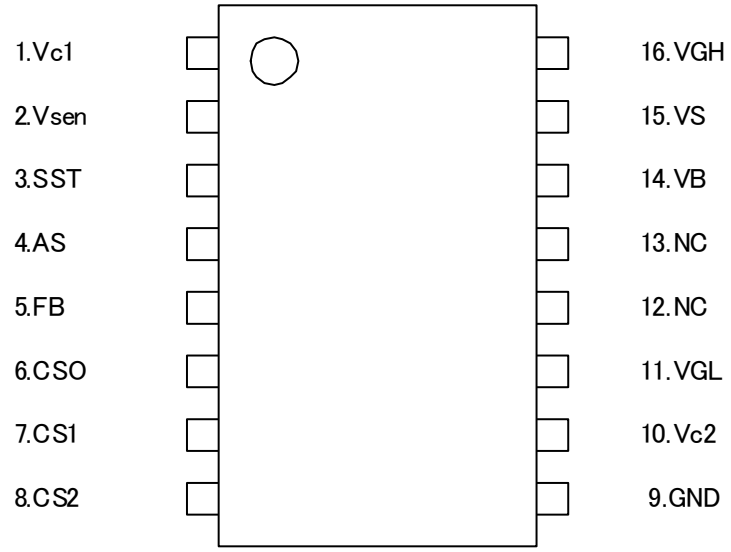


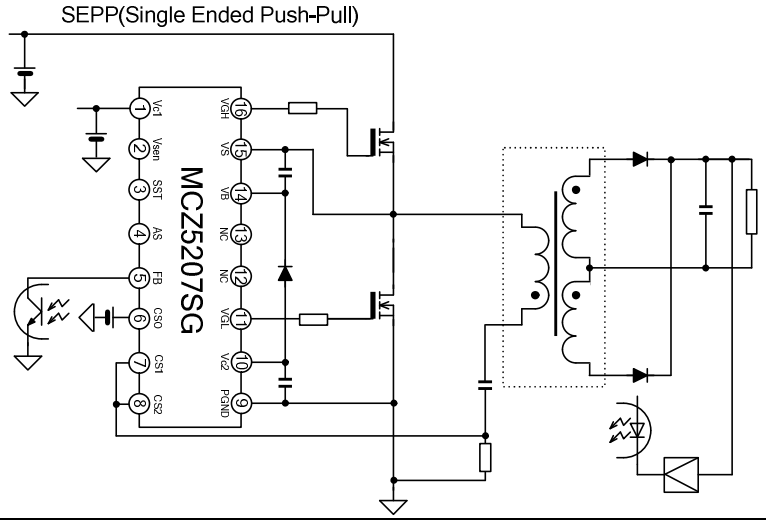
Fig 2 . MCZ5207SG pin assignment

1.4 Functions

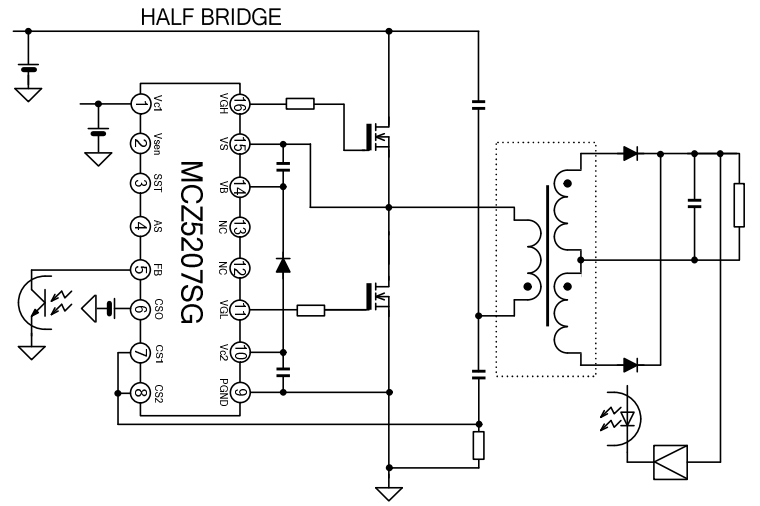
Pin number	symbol	description
1	**Vc1**	IC supply voltage VCC input up to 35V UVLO(on) = 12.9V / UVLO(off) = 8.7V.
2	**Vsen**	Bus **V**oltage **sen**sing input For brown-out protection and on/off with external signal
3	**SST**	**S**oft **S**tart and **T**imer delayed latching protection timing capacitor connecting terminal Latching protection with external signal is supported.
4	**AS**	**A**ctive **S**tdby / burst operation signal input
5	**FB**	**F**eed **B**ack signal input / timing capacitor and resistor connecting terminal F(min) / f(ss) / initial dead time is determined
6	**CSO**	Frequency clamp **C**urrent **S**ensing comparator **O**utput Averaged OLP response is determined.
7	**CS1**	**C**urrent **S**ensing input for shorted load protection Peak current limiting sensing threshold voltage is +/- 0.5V.
8	**CS2**	**C**urrent **S**ensing input for frequency clamp and capacitive mode protection Protection point can be adjusted independently of CS1. +/- 0.5V threshold for frequency clamp and +/- 0.1V for anti capacitive mode protection.
9	**GND**	IC Ground terminal
10	**Vc2**	Stabilized VDD output for gate drive 10.2V
11	**VGL**	**G**ate drive output for **L**ow side switch
12-13	**NC**	Not connected
14	**VB**	**B**ootstrapped floating VDD input for high side gate driver
15	**VS**	Floating driver reference voltage (= source terminal of high side switch)
16	**VGH**	**G**ate drive output for **H**igh side switch

1.5 Applicable circuit configuration

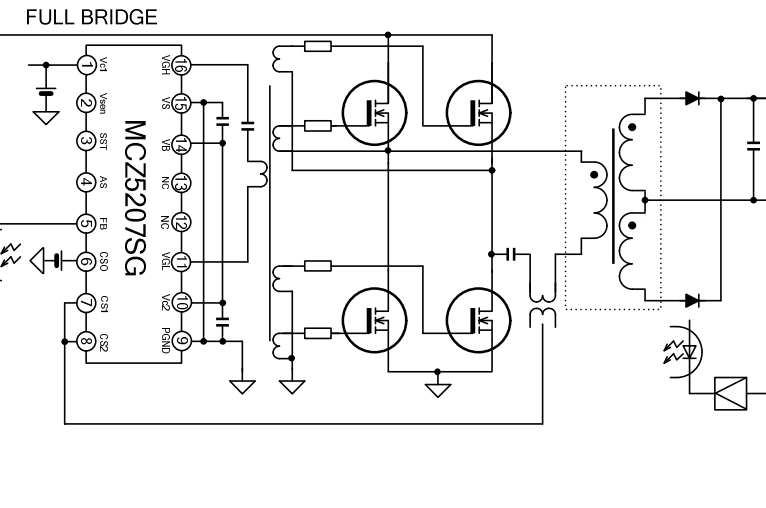
Most simple SEPP(Single Ended Push-Pull)



Input ripple current reduction (Half Bridge)



For high power application (Full Bridge)



2 Functional description

2.1 Operation mode

MCZ5207SG operation timing chart is shown in **2.2** and **2.3**.
Method of selecting components value is described in article **3**.

MCZ5207SG has three operation mode :

1) Normal operation mode
2) Active stdby mode
3) Burst operation mode

Normal operation is assumed in this document unless otherwise specified.
Active stdby mode and burst mode operation details are described in **2.3.11** and **2.3.12**.

2.2 Supply voltage

2.2.1 IC main supply (Vc1)

Vc1 UVLO threshold is 12.9V (start) and 8.7V (stop).
When **Vc1** terminal voltage reaches to **Vc1(start) 12.9V**, **Vc2** output is enabled and IC operation starts. When **Vc1** terminal voltage decreases to less than **Vc1(stop) 8.7V**, **Vc2** output is disabled and IC operation stops. Latching protection is initialized when **Vc1** terminal voltage decreases to less than **Vc1(latch reset) 8.3V**.

2.2.2 Stabilized gate drive VDD (Vc2)

Vc2 terminal is an output of internal **10.2V** dropper for the gate driver. **Vc2** output is also a voltage source of boot strapping high side VDD. Filtering capacitor should be placed close to **Vc2** - GND. Please be noticed that gate driving ripple current flows in this **Vc2** filtering capacitor, so take care of capacitor ripple current rating.

Vc2 output is enabled when **Vc1** reaches to **Vc1(start) 12.9V**. Internal oscillator starts operation when **Vc2** terminal voltage reaches to **Vc2(start) 9.6V** and Gate drive output is enabled.
Refer to article **2.3** to see gate drive output timing.

2.2.3 Boot strapped High side floating VDD (VB)

VB is the input from **Vc2** voltage source through boot strapping diode. Please place boot strap filtering capacitor close to **VB** – **VS** terminal. 600V fast and soft recovery FRD like **D1NK60** (axial) or **D1FK60** (SMD) is recommended as a boot strapping diode, snappy recovery type should not be chosen
High side UVLO is implemented watching **VB** – **VS** terminal voltage. **VB-VS(start)** is **7.3V** and **VB-VS(stop)** is **5.1V**. Undesired linear operation can be prevented by this independent high side VDD UVLO.

2.3 Functional terminal detail

2.3.1 Gate drive output (VGL and VGH)

Gate driver output terminals are **VGL** (Low side MOSFET) and **VGH** (High side MOSFET) with 0.18Apk sourcing and 0.4Apk sinking capability. Generic gate drive connection is shown in **Fig.3(A).** Large Qg gate can be handled with additional sinking diode shown in **Fig.3(B),(C).**
In this case snappy recovery diode is not recommended. Soft recovery fast switching or SBD is recommended like **D1NS4** (40V axial SBD) or **M1FM3** (30V SMD SBD).

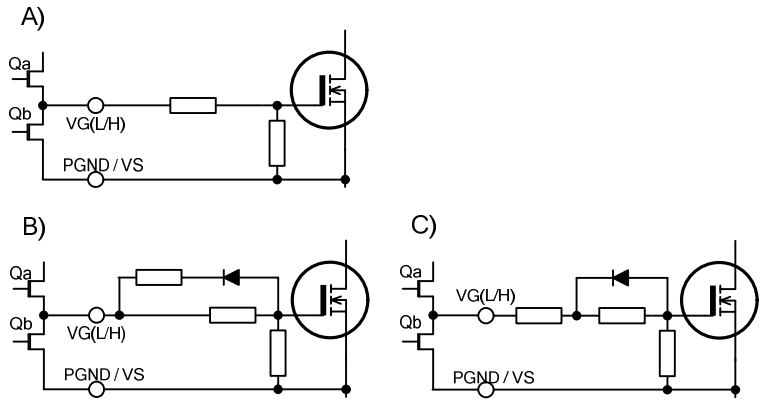


Fig. 3 . Gate drive circuits

2.3.2 Oscillator (FB)

The timing of gate drive pulse **VGL** and **VGH** is determined by charging and discharging time period of timing capacitor **Ct** (connected between **FB** and GND).
Gate output is enabled during **Ct** discharging period. **VGL** and **VGH** are alternately outputted to drive each gate of MOSFETs. During **Ct** charging period, both **VGL** and **VGH** are simultaneously disabled to prevent shoot through of MOSFETs, this time period is known as Dead time (**DT**),.
DT is depend on **Ct** and **Rt** value. Please refer to electric characteristics charts

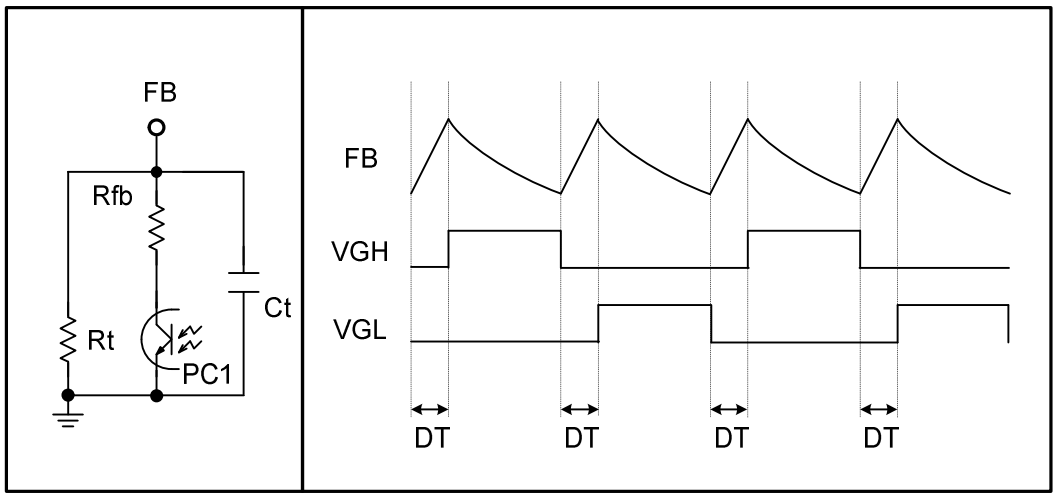


Fig.4 . FBL – VGL/VGH timing

Operating frequency is varied by controlling **Ct** discharging current. (**Fig.5)**
Dead time expands according to operating frequency increase, thus **ZVS** (Zero Voltage Switching) operation can be easily achieved in wide input/output range and various resonant condition.
Minimum operating frequency (**fmin**) is determined by timing capacitor **Ct** and timing resistor **Rt**.
Maximum operating frequency (**fmax**) is determined by **Ct** ,**Rt** and **Rfmax** connected in series to **FB** control loop.
Less than 500kHz is recommended in continuous operation.
Soft starting frequency (**fss**) is determined by **Ct** value, **fss** and **fmax** is independent so undesired frequency increase can be avoided under heavy CCM LLC operation.

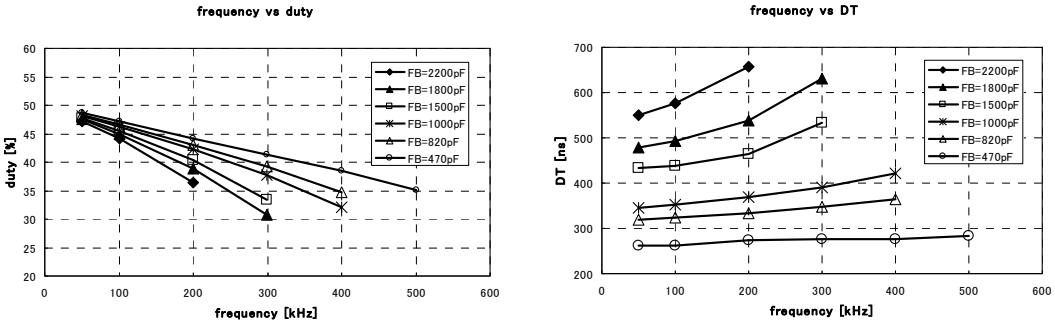


Fig. 5 . Gate output duty/dead time vs frequency

2.3.3 Brown-out protection (Vsen)

Vsen terminal monitors the input bus voltage and determines **Csst** discharge ON/OFF according to Vsen terminal voltage. This input UVLO function prevents excessive resonant rush current flow and capacitive mode operation under various input brown-out condition.

Timing chart of **Vsen** brown-out protection is shown in **Fig. 6**
Under input bus voltage increasing condition , **Csst** starts to be charged when Vsen terminal voltage reaches to **Vsen1(ss-reset) 3.55V** and Gate output is enabled when SST terminal voltage reaches to **Vss(st) 0.6V**. Operating frequency decreases according to SST terminal voltage increases.
And under input bus voltage decreasing condition, **Csst** starts to be discharged when **Vsen** terminal voltage decreases to **Vsen2(ss-reset) 3.25V**. Operating frequency increases gradually according to SST terminal voltage decreases and Gate output is disabled when **SST** terminal voltage reaches to less than **Vss(sp) 0.5V**.
Vsen brownout threshold voltage is switched automatically according to **AS** terminal voltage status.

Normal operation (**AS OFF**) : **Vsen** ON 3.55V / **Vsen** OFF 3.25V
AS operation mode (**AS ON**) : **Vsen** ON 1.0V / **Vsen** OFF 0.9V
Burst operation mode : **Vsen** ON 1.0V / **Vsen** OFF 0.9V

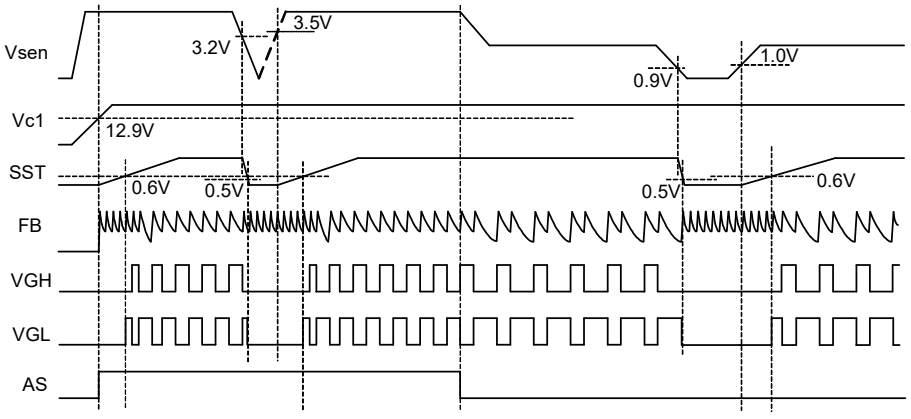


Fig. 6 . Brown-out protection timing

2.3.4 Dynamic peak current limiting OCP (CS1)

Shorted load protection (**OCP1**, hereinafter) is a fast response cycle by cycle peak current limiter. When **CS1** terminal voltage reached to **CS1** threshold (+/- 0.5V), gate drive output is disabled instantaneously and **Ct** and also **Csst** starts to be charged . 0.5V threshold is low enough so sensing loss is not high even when using current sensing resistor method.

Fig. 7 shows the timing charts of **OCP1** operation and **Csst** charging detail is described in article **2.3.8.**

LEB is enabled during **FB(top) 4.65V** to **4.4V** time period. So even heavy non-ZVS surge current cannot trigger **OCP1**. From **OCP1** detection to **Ct** charging has 200nsec time delay due to internal filter.

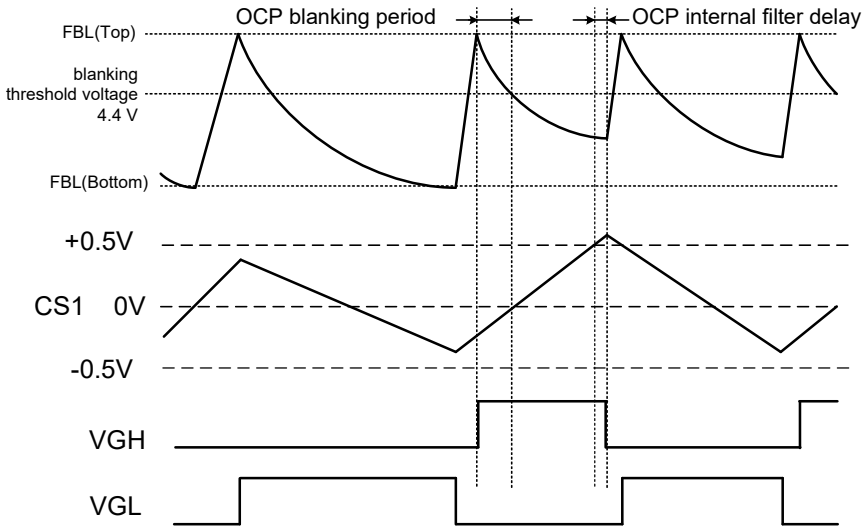


Fig. 7 OCP1 operation timing

2.3.5 Frequency clamped averaging OLP (CS2 and CSO)

The **MCZ5207SG** has frequency clamped Over Load Protection (**OCP2**, hereinafter). When **CS2** terminal voltage reaches to **+/-0.5V**, **CSO** starts to be charged and operating frequency increases according to **CSO** terminal voltage increases. Operating frequency and **CSO** terminal voltage is shown in **Fig. 8**

Please be noticed that **OCP2** operating point is independent from **OCP1**, so desired operating point can be adjusted.

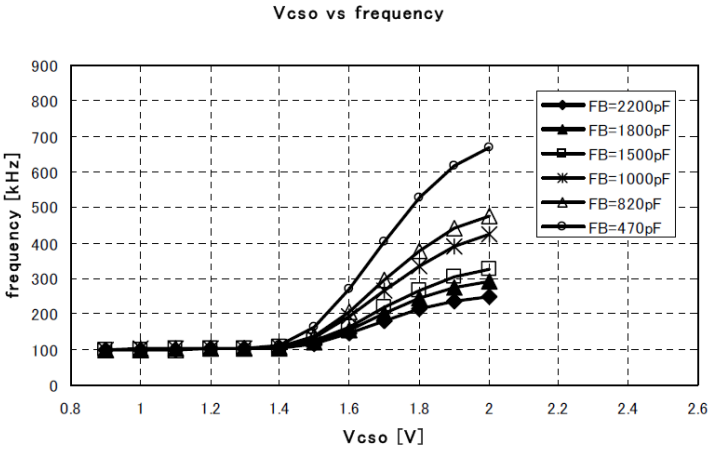


Fig.8 Operating frequency vs CSO terminal voltage

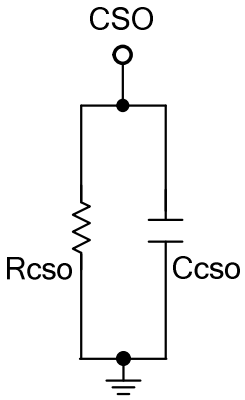


Fig. 9 CSO terminal

2.3.6 Anti-Capacitive mode protection (CS2)

The **MCZ5207SG** adopts anti-capacitive mode protection to prevent damgerous MOSFET body diode di/dtoperation. When **CS2** terminal voltage crosses **Vdi/dt(+/-) +/- 0.1V** before expected gate turn off , gate output is instantaneously disabled. (shown in **Fig.10**)

During high side MOSFET ON period, high side gate turns off and **Ct** starts charged immediately when **CS2** terminal voltage reaches to **+0.1V** in negative direction.And during low side MOSFET ON period, low side gate turns off and **Ct** starts to be charged when **CS2** turminal voltage reaches to **-0.1V** in possitive direction.
To prevent malfunction caused by switching surge voltage , capacitive mode protection is disabled during VFB > **VFB(msk) 4.4V .** Even if **CS2** terminal voltage crosses this threshold during this time period, anti-capacitive mode protection does not work.

Timer delayed latching protection is enabled only when LLC is operating in **AS** mode.

- Normal and burst mode : **Csst** will not be charged in anti-capacitive mode protection
- AS mode : **Csst** will be charged during anti-capacitive mode protection operates.

This anti- capacitive mode protection results in LLC operating always in above ZVS region, so feedback - control turnaround never occurs.

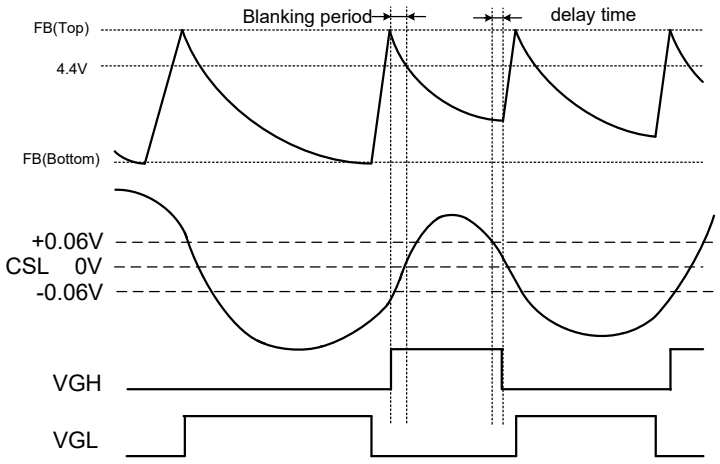


Fig. 10 . Anti-capacitive mode protection timing

2.3.7 Safe-startup protection (Tss(3))

The **MCZ5207SG** has another di/dt protection at startup period to prevent too fast turn-off before body diode conduction period ends.
On 2nd **VGL** output period, **VFB (bottom)** threshold voltage is switched to lower value and results in increase of ON time period . Timing chart is shown in **Fig.11**.

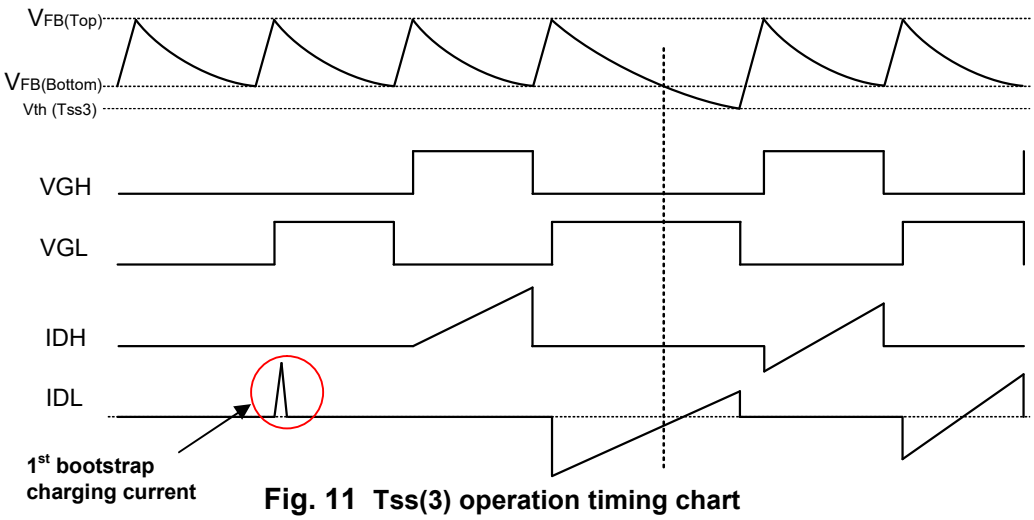


Fig. 11 Tss(3) operation timing chart

2.3.8 Soft start (SST)

During starting period , operating frequency decreases from soft start frequency (**fss**) to stabilized frequency proportionally to **SST** terminal voltage to prevent excessive resonant current or output inrush current and capacitive mode operation.
Csst starts to be charged under two conditions as below :

1. **Vc1** > **Vc1(start) 12.9V** AND
2. **Vsen** terminal voltage > **Vsen1(ss-reset) or Vsen3(ss-reset)**

Oscillator starts operation at **Vsst** = 0.6V and operating frequency is stabilized before **Vss**t reaches to **Vss(open) 2.1V**. **Fig.12** shows frequency and **Vsst** characteristics .

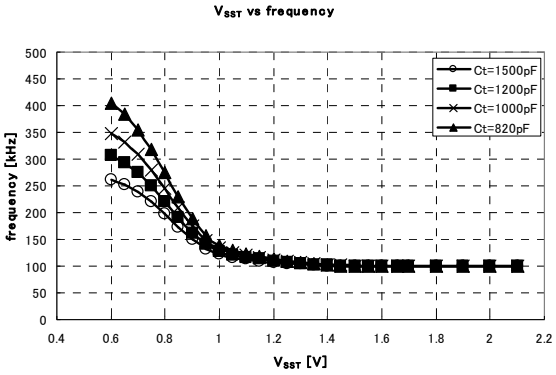


Fig. 12 Operation frequency and SST terminal voltage

2.3.9 Timer delayed latching protection (SST)

Csst also functions as latching protection timing capacitor.
SST terminal capacitor **Csst** starts to be charged in two condition as following:

1. **OCP1** or **OCP2** operates continuously OR
2. Anti-capacitive mode protection operates in **AS** mode.

When **Csst** is charged continuously and **SST** terminal voltage reaches to **Vtimer(set) 3.5V**, long interval intermittent protection starts. After specified time period, normal operation restarts when abnormal condition was removed. If abnormal condition has not been removed, IC enters into latched off mode after second intermittent operation finished.

To initialize latching status, restart **Vc1** to **Vc1<8.3V**.

Protection timing chart is shown in **Fig.13**. **Csst** charging current is depend on **CSO** terminal voltage during continuous **OCP2** operation.

Table 1. Csst charging current

Protection status		Csst charging current
OCP1		40uA
OCP2	1.0V < Vcso < 1.75V	1.9uA
	Vcso 1.75V	40uA
Anti-capacitive (during AS mode)		40uA

Internal latching counter is initialized in two conditions as following:

1) **Vsst** decreases to 2.1V (recovered to normal operation)
2) **Csst** discharging condition (**Vc1** ON/OFF, **Vsen** on/off)

Latching counter initialization helps to avoid undesirable latching. When abnormal condition is counted twice, IC enters into latched stop mode.

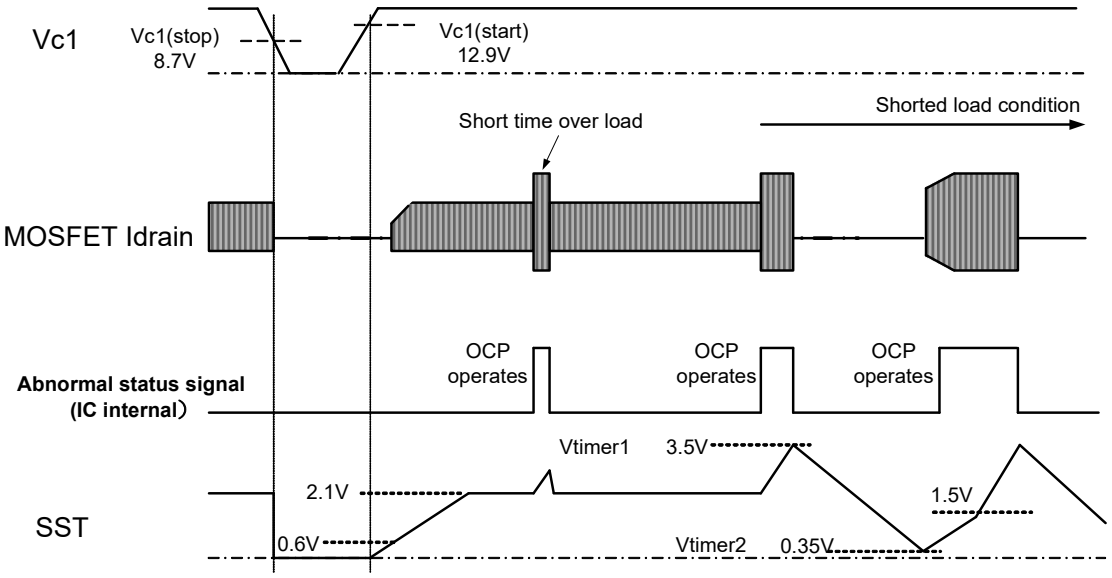


Fig. 13 Csst timing chart

2.3.10 Boot strapping circuit

High side floating VDD (**VB**-**VS**) capacitor is charged during conduction period of low side MOSFET as shown in **Fig.14**.

VB – **VS** voltage is simply equals to (**Vc2** – **Vf** of Dboot). Although very stable operation is possible due to stabilized **Vc2** voltage, if huge negative surge voltage superimposed to **VB**, please add zener diode clamp of 15V to avoid high side logic malfunction. This surge voltage is caused by parasitic inductance in main switching loop and huge turn off current .

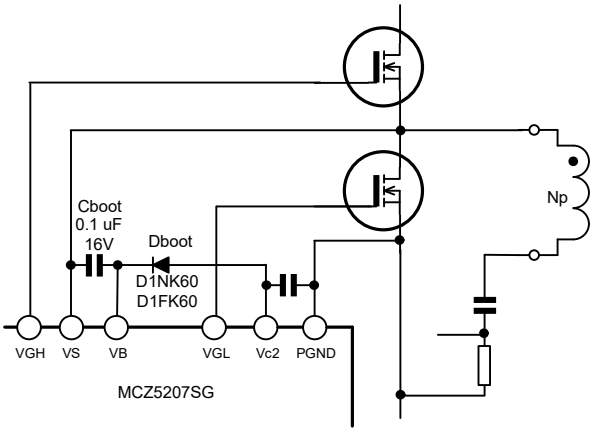


Fig. 14 Boot Strapping circuit

2.3.11 Active stdby asymmetric operation (AS)

The **MCZ5207SG** has asymmetric operation mode called **Active Standby Mode** to improve light load efficiency. When **AS** terminal voltage less than **Vas(on) 0.8V**, operation enters into asymmetric operation mode. After entering in **AS** mode, operation will return to normal symmetric operation mode when AS terminal voltage reaches to more than **Vas(off) 1.0V.** To avoid undesirable **AS** mode operation, add 1nF – 10nF closed to **AS** terminal. (Even when **AS** function is not used, add filtering capacitor .)
AS terminal open voltage is 2.5V.
Circuit configuration is shown in **Fig. 15.**

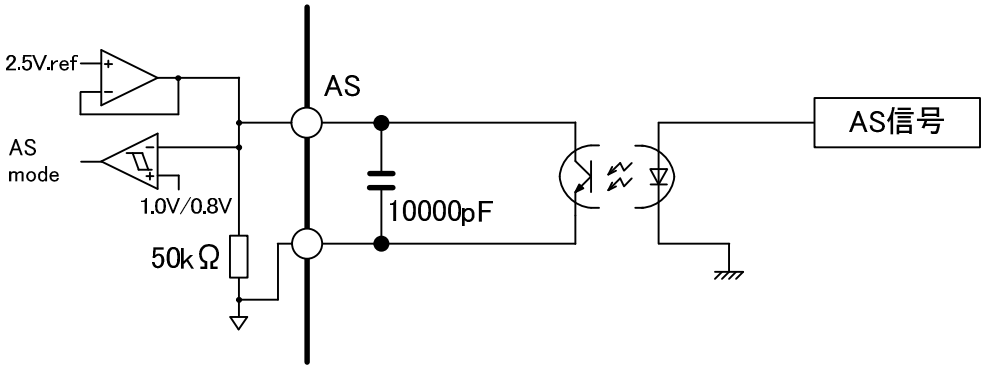


Fig. 15 AS signal configuration example

When **AS** signal is not applied (**Vas(open) 2.5V), VGH** and **VGL** output is symmetrically 50% duty cycle, and if **AS** terminal is pulled down externally to less than 2.2V, **Ct** charging threshold of low side MOSFET starts decreasing. This threshold decreasing is proportional to **AS** terminal voltage and finally reaches to bottom value of threshold when **AS** terminal voltage reaches to 1.0V. Decreasing of **Ct** discharging threshold results in **VGL** pulse width increasing. Maximum duty unbalance is 1:2 (**VGH** : **VGL**).

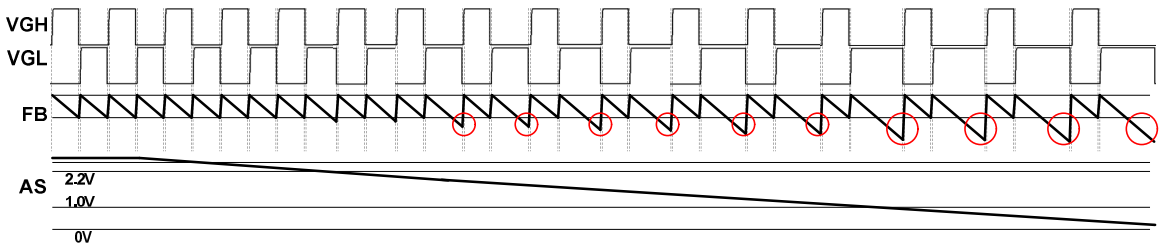


Fig. 16 Asymmetric Gate output example

When operation is switched to **AS** mode,

- **Vsen** threshold (**SS**-Reset) is switched from **3.55V/3.25V** to **1.0V/0.9V**.
- **Csst** charging enabled if anti-capacitive protection operates.

2.3.12 Burst mode operation (AS)

BURST mode operation starts when more than 4.5V external voltage is applied to **AS** terminal. **Csst** is discharged to 0.5V that results in gate output disabled. And when **AS** terminal voltage decreases to 4.0V , **Csst** starts to be charged and starting cycle begins. During burst mode operation, **Csst** charging current is switched from 30uA to 60uA to shorten starting time period. Also Vsen threshold voltage is switched to 1.0V(on) / 0.9V(off) preparing to PFC stopped LLC operation. Operation will recover to normal continuous operation when **AS** terminal voltage decreases to 3.0V or less.

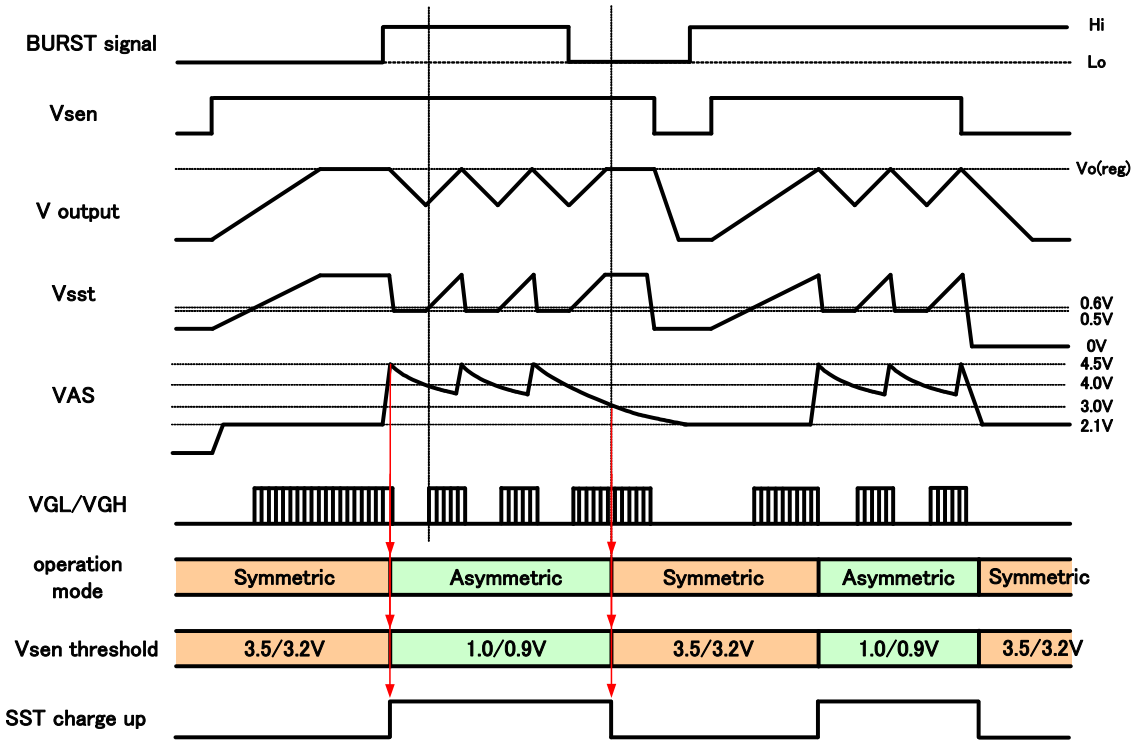


Fig. 17 Burst mode operation timing

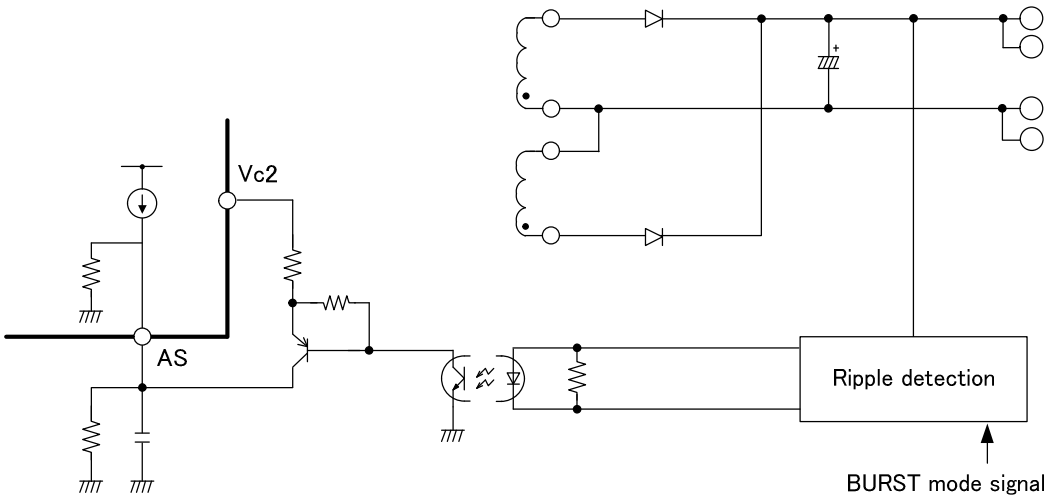


Fig. 18 BURST w/external signal configuration example

2.4 Thermal shut down protection (TSD)

The MCZ5207SG implements Thermal Shut Down protection. Threshold temperature is **TSD 140°C** min. with **40°C** hysteresis. During **TSD** mode, IC operation entirely stops.

3 Selecting components value

3.1 Input Brown out protection (Vsen)

Vsen SS reset threshold voltage is **3.55V/3.25V**. (**AS** mode OFF)
1.0V/0.9V. (**AS** mode ON)
Vsen terminal sink current is less than **0.2uA**,so **20uA** or more sensing bias current is recommended not to be affected by the sink current.
Connect a capacitor of **1000** to **10000pF** between **Vsen** and **GND** for filtering.

Low side resistor, **RvsenseL(init)** is obtained from **formula (1)**. Correct value of **Vbulkreset** threshold is obtained from **formula (2)** using actual value of **RvsenseL**.
In **AS** mode operation, use **formula (3)**.

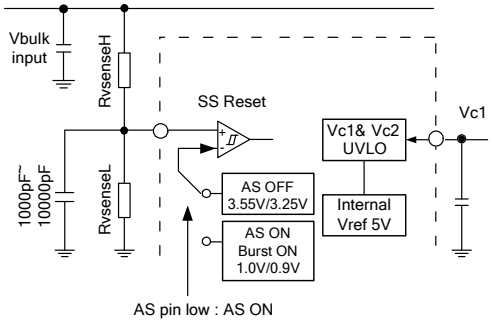


Fig. 19 Vsen internal block

$$R_{VsenceL\ (init)} = \frac{3.25 \times R_{VsenseH}}{V_{bulkreset} - 3.25} \quad \cdots (1)$$

$$V_{bulkreset} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 3.25 \quad \cdots (2)$$

$$V_{bulkreset\ (AS\ ON)} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 0.9 \quad \cdots (3)$$

3.2 Oscillator / Feedback (FB)

Operating frequency can be controlled by pulling current from **FB** terminal. **Ct** , **Rt** and **Rfb** connected to **FB** terminal determine minimum frequency (**fmin**),maximum frequency (**fmax**) , starting frequency (**fss**) and dead time (**DT**).

3.2.1 dead time and soft start frequency (Ct)

Dead time and soft start frequency **fss** are determined by **Ct** capacitance. Select **Ct** capacitance from characteristic specification sheet.
Capacitance value of **Ct** of 470pF to 2200pF is recommended due to the relation with dead time.

3.2.2 Minimum frequency fmin (Rt resistance)

Minimum frequency **fmin** is determined by **Rt** value. (Connect between **FB** and **GND**.) Relation between **Rt** resistance and frequency is shown in characteristic specification sheet.
The estimated value of **fmin** is obtained from formula (4) to (6). **tcharge** is a dead time and **tdischarge** is ON time period of **VGL**/**VGH**.
Calculated value is an estimated value including small error due to comparator delay time of around 100nsec. (**VFBL(bottom)** : 3.5V , **VFBL(top)** : 4.65V)

$$t_{charge} = \frac{Rt \times Ct \times VFB_{(top)}}{Rt \times 7.0 \times 10^{-3} - VFB_{(top)}} - \frac{Rt \times Ct \times VFB_{(bottom)}}{Rt \times 7.0 \times 10^{-3} - VFB_{(bottom)}} \quad \text{---- (4)}$$

$$t_{discharge} = -Rt \times Ct \times \ln \frac{VFB_{(bottom)}}{VFB_{(top)}} \quad \text{---- (5)}$$

$$f_{\min} = \frac{1}{2 \times \left(t_{charge} + t_{discharge} \right)} \quad \text{---- (6)}$$

3.2.3 Maximum frequency fmax (FB resistor)

Maximum frequency **fmax** is determined **Rt** and **Rfb** value.
Check the characteristic specification sheet and determine the maximum frequency.

3.3 Soft start / Timer delayed protection (SST)

Soft start charging current **Iss(charge)** is **30uA**. When **SST** voltage rises to **0.6V**, gate output starts and timer charging is enabled when **SST** voltage rises to **1.5V**.
Soft starting time **tss** is a time period in which SST voltage rises from **0.6V** to **1.5V**.
tss is obtained from **formula (7)**.
Operating frequency and

$$t_{ss} = \frac{0.9 \times C_{ss}}{30 \times 10^{-6}} \quad \cdots(7)$$

Timer charging current **Itimer(charge)1** is **40uA** and output disable threshold voltage is **3.5V**.
Thus, Timer charging time **ttimer** is obtained from **formula (8)**.

$$t_{timer} = \frac{1.4 \times C_{ss}}{40 \times 10^{-6}} \quad \cdots(8)$$

Timer charging current is different when **OCP2** is operating. If **CSO** terminal voltage is less than 1.75V, charging current **Itimer(charge)2** is **1.9uA**,so time period to operation stop (**VSST**=3.5V) **Ttimer** is obtained from **formula (9)**.

$$t_{timer} = \frac{1.4 \times C_{ss}}{1.9 \times 10^{-6}} \quad \cdots(9)$$

If **CSO** terminal voltage is grater than1.75V, charging current **Itimer(charge)3 = 40uA** ,so time period to operation stoop Ttimer is obtained from **formula (8)**.

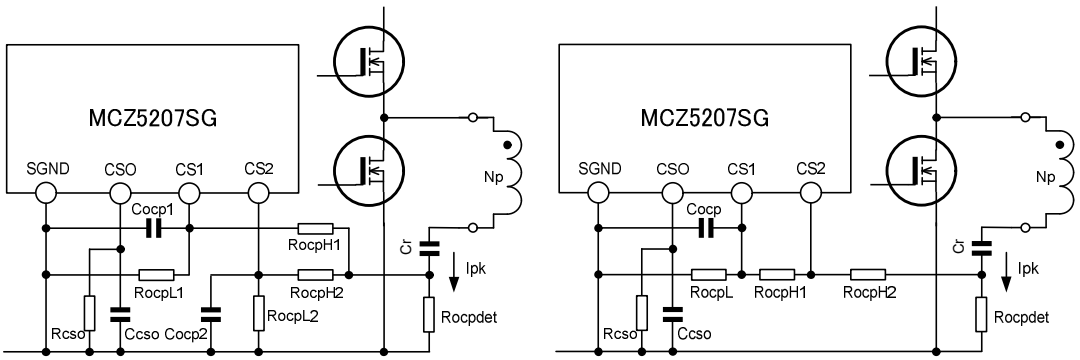
Csst discharging current **Itimer(discharge)** is **6.5uA** and operation restarts when **SST** terminal voltage decreases to less than **Vtimer(reset) 0.35V .** So gate output disabling time period is obtained from **formula (10)**.

$$t_{timer(dis)} = \frac{3.15 \times C_{ss}}{6.5 \times 10^{-6}} \quad \cdots(10)$$

3.4 OCP1/OCP2 and anti-capacitive mode protection (CS1/CS2)

Current sensing connection example is shown in **Fig.20**
Type **(a)** is **CS1/2** independent sensing and **(b)** shows **CS1/2** common sensing connection.
Generally **OCP2** operating point is lower than **OCP1's** . In this condition **OCP2** stabilizes LLC operating frequency in transient over load / peak load condition and **OCP1** finally halts entire LLC operation in shorted load condition.

Current sensing resistor **Rocpdet** is calculated from desired **OCP** threshold **Ipk** using **formula (11)**.
When the connection is assumed as type(a) , tentative value of **RocpL(init)** is obtained from **formula(12)** and correct value of resonant current peak **Ipk(ACT)**is calculated from **formula(13)** using actual value of **RocpL.**
Considering **CS1/2** terminal sourcing current 95uA, 10 – 47 ohm is recommended for **RocpH**.
CS2 terminal sensing voltage is also used for ant-capacitive mode protection. CS2 operating point should be determined considering **+/-0.10V** capacitive mode protection threshold.
Connect filtering capacitor of 1nF to 10nF close to CS1 or CS2 terminal to suppress OCP malfunction.
Frequency stabilized OLP (OCP2) realizes smooth constant power output characteristics and resonant current envelope, they are very suitable for Audio amp or huge peak current flowing application. Actual example of output characteristics is shown in **Fig.21.**
Please be noticed that setting CS2 operating point to too high level causes undesirable anti-capacitive mode protecting operation in normal load condition.



(a) CS1/2 independent sensing **(b) CS1/2 common sensing**

Fig. 20 CS1 and CS2 current sensing circuit

$$R_{ocp\,det(init)} > \frac{0.5}{Ipk} \quad [ohm] \quad \cdot\cdot\cdot(11)$$

$$R_{ocpL(1/2)} = \frac{0.5 \times R_{ocpH(1/2)}}{Ipk \times R_{ocp\,det} - 0.5} \quad [ohm] \quad \cdot\cdot\cdot(12)$$

$$I_{pk(ACT)} = \frac{R_{ocpH(1/2)} + R_{ocpL(1/2)}}{R_{ocpL(1/2)} \times R_{ocp\,det}} \times 0.5 \quad [A] \quad \cdot\cdot\cdot(13)$$

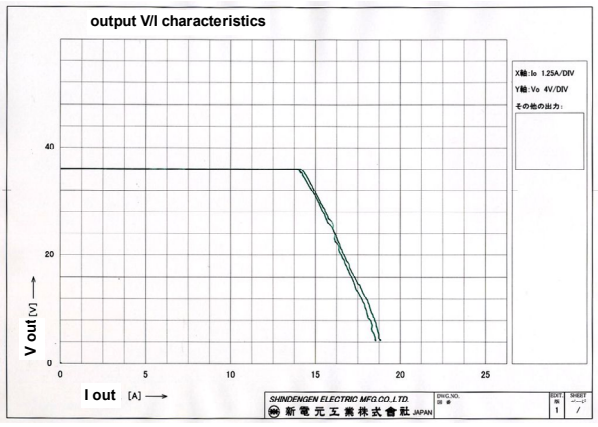
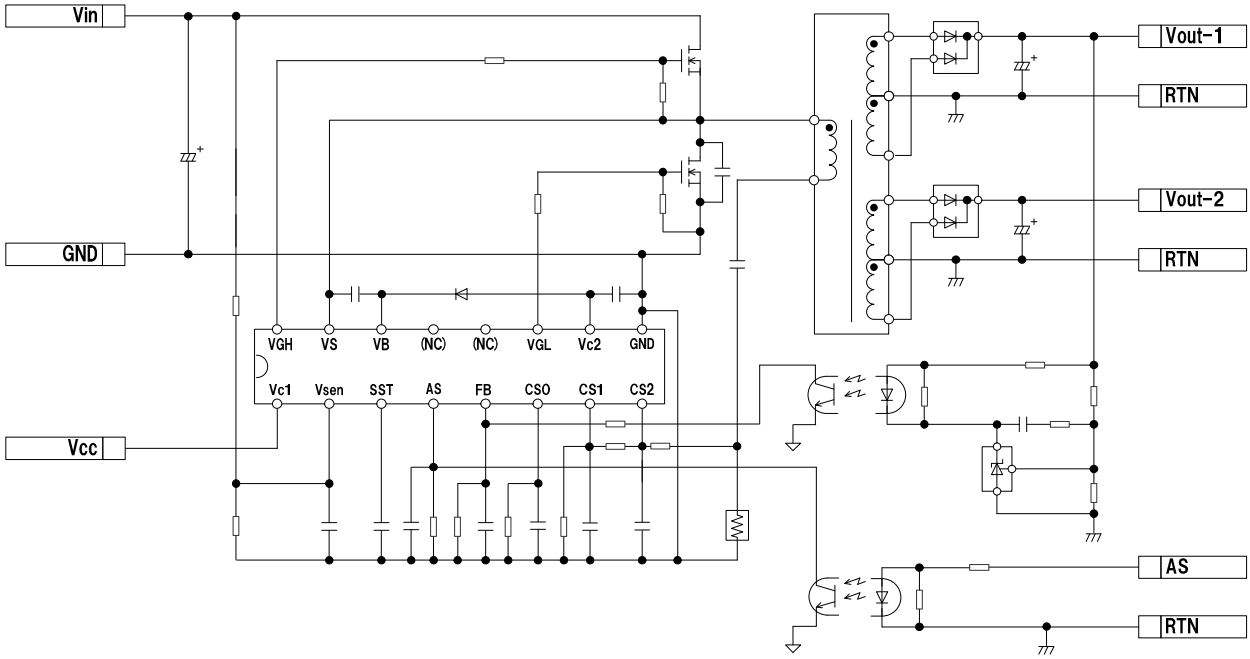


Fig. 21 OLP characteristics example

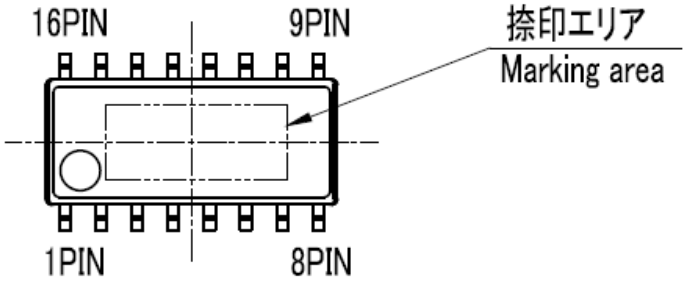
4 Circuit diagram

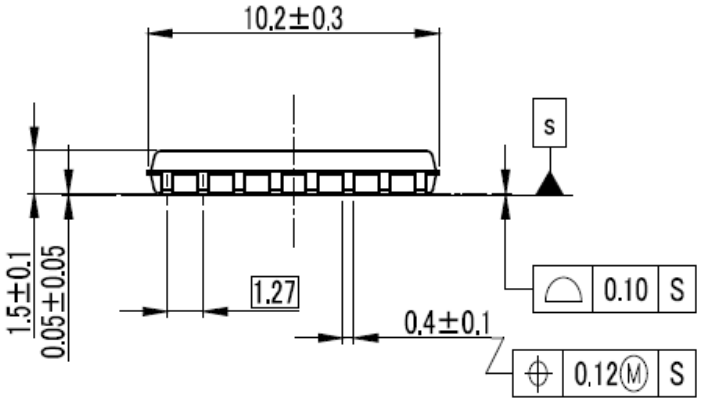
4.1 Configuration example of DC to DC dual output LLC

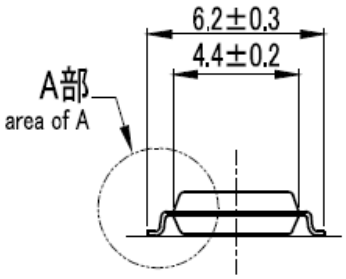


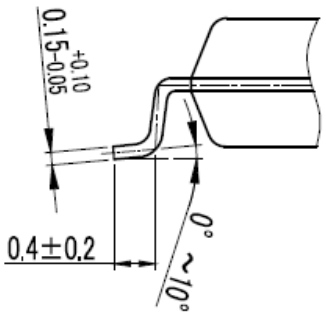
5 Dimension

5.1 SOP16 (MCZ5207SG)









A部詳細図
Detail area of A

Notes: